Product Specification

Part Name: OEL Display Module

Customer Part ID:

Part ID: GME64128-01

Ver: A

Customer:
Approved by

From: GoldenMorning Electronic
Approved by

Revised History

Part Number	Revision	Revision Content	Revised on
GME64128-01	V1.0		20171127

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Revision History
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1. Basic Specifications

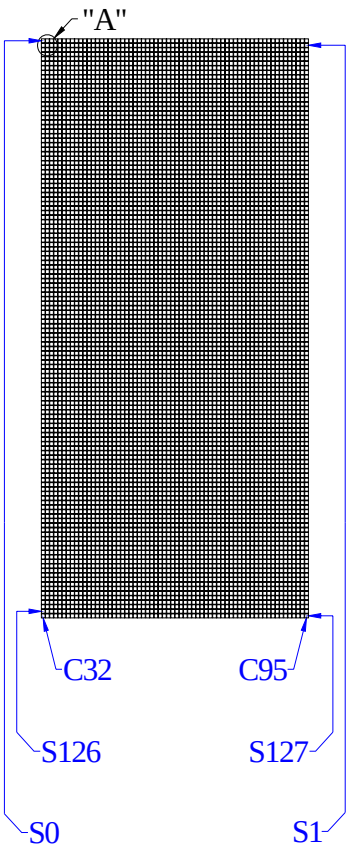
1.1 Display Specifications

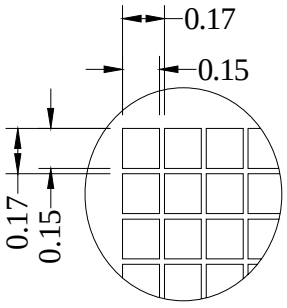
1) Display Mode: Passive Matrix
2) Display Color: Monochrome (White)
3) Drive Duty: 1/128 Duty

1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing
2) Number of Pixels: 64 × 128
3) Panel Size: 17.1 × 35.8 × 1.43 (mm)
4) Active Area: 14.7 × 29.42 (mm)
5) Pixel Pitch: 0.17 × 0.17 (mm)
6) Pixel Size: 0.15 × 0.15 (mm)
7) Weight: TBD

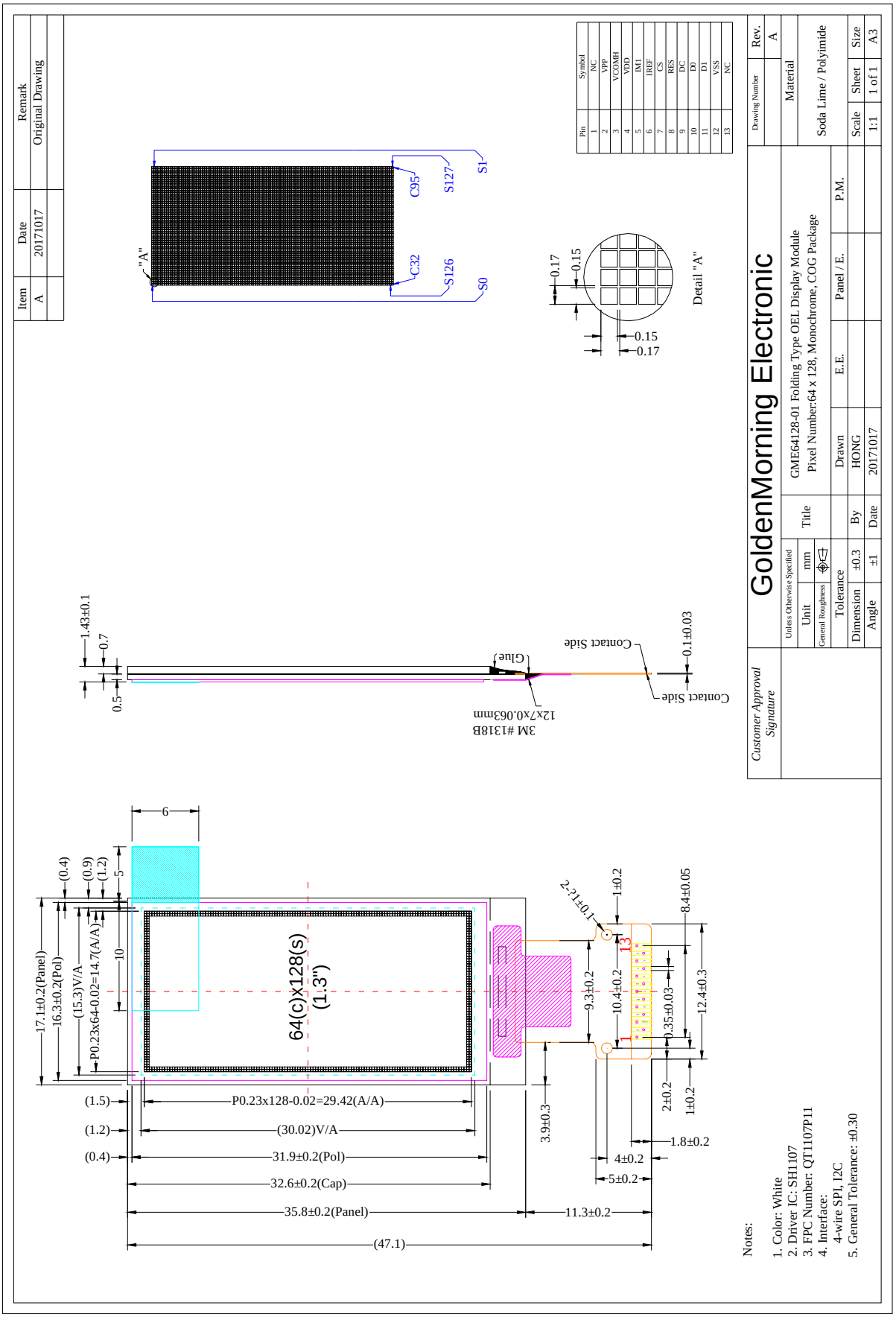
1.3 Active Area / Memory Mapping & Pixel Construction





Detail "A"
Scale (10:1)

1.4 Mechanical Drawing



1.5 Pin Definition

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Power Supply</td></tr>
<tr><td>2</td><td>VPP</td><td>P</td><td>Power Supply for OEL Panell
This is the most positive voltage supply pin of the chip. It must be supplied externally.</td></tr>
<tr><td>4</td><td>VDD</td><td>P</td><td>Power Supply for Logic
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>12</td><td>VSS</td><td>P</td><td>Ground of OEL System
This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.</td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td colspan="4">Driver</td></tr>
<tr><td>6</td><td>IREF</td><td>I</td><td>Current Reference for Brightness Adjustment
This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 12.5μA maximum.</td></tr>
<tr><td>3</td><td>VCOMH</td><td>O</td><td>Voltage Output High Level for COM Signal
This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V_{SS}.</td></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>5</td><td>IM1</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>IM1</td></tr>
<tr><td>4-wire SPI</td><td>0</td></tr>
<tr><td>I2C</td><td>1</td></tr>
</table></td></tr>
<tr><td>8</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>7</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>9</td><td>A0</td><td>I</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register.
When the pin is pulled high and serial interface mode is selected, the data at SI will be interpreted as data. When it is pulled low, the data at SI will be
transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.
For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>10,11</td><td>D0,D1</td><td>I/O</td><td>Serial Data Input/Output and clock
When serial mode is selected, D1 will be the serial data input SI and D0 will be the serial clock input SCL.
When I2C mode is selected, D1 be the serial data input SDA and D0 is the serial clock input, SCL.</td></tr>
<tr><td colspan="4">Reserve</td></tr>
<tr><td>1,13</td><td>NC</td><td>-</td><td>Reserved Pin
The N.C. pins between function pins are reserved for compatible and flexible design.</td></tr>
</table>

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	3.6	V	1, 2
Supply Voltage for Display	V_{PP}	7	16.5	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (150 cd/m^2)		10,000	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: End of lifetime is specified as 50% of initial brightness reached. The reference average operation life time at room temperature is estimated by the accelerated at high temperature conditions.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (V_{PP} Supplied Externally)	L_{br}	Note 4	120	160	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.27	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	>10000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{PP} = 9V.
Software configuration follows Section 4.5 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.5	V
Supply Voltage for Display	V_{PP}	Note 5	8.5	9.0	9.5	V
High Level Input	V_{IH}	I_{OUT} = 100μA, 3.3MHz	$0.8\times V_{DD}$	-	V_{DD}	V
Low Level Input	V_{IL}	I_{OUT} = 100μA, 3.3MHz	0	-	$0.2\times V_{DD}$	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	$0.8\times V_{DD}$	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	$0.2\times V_{DD}$	V
Operating Current for V_{CI}	I_{DD}		-	55	100	μA
Operating Current for V_{PP}	I_{PP}	Note 6	-	24	29	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	0.1	5	μA
Sleep Mode Current for V_{PP}	$I_{PP, SLEEP}$		-	0.5	5	μA

Note 5 & *6*: Brightness (L_{br}) and Supply Voltage for Display (V_{PP}) are subject to the change of the panel characteristics and the customer's request.
Note 6: VDD = 2.8V, VPP = 9.0V, 100% Display Area Turn on.

* Software configuration follows Section 4.5 Initialization.

3.3 AC Characteristics

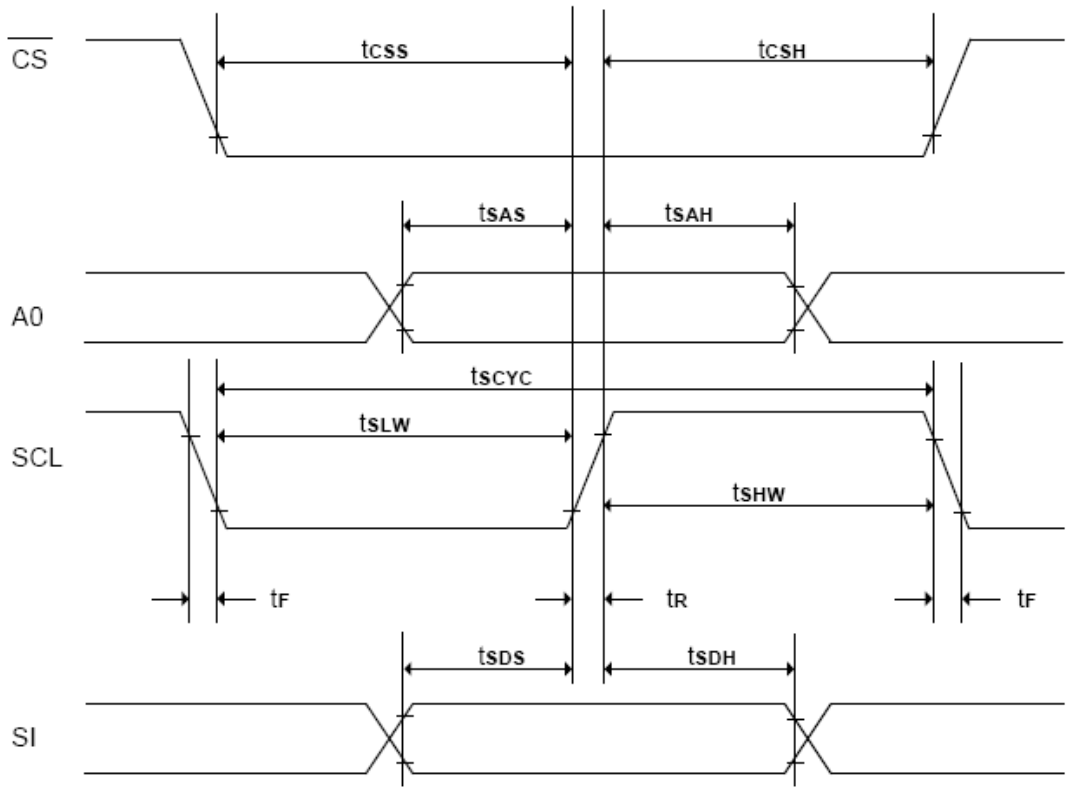
3.3.3.1 Serial Interface Timing Characteristics: (4-wire SPI)

(V_{DD} - V_{SS} = 1.65V to 2.4V, T_a = 25°C)

Symbol	Description	Min	Max	Unit
t_{SCYC}	Serial Clock Cycle Time	500	-	ns
t_{SAS}	Address Setup Time	300	-	ns
t_{SAH}	Address Hold Time	300	-	ns
t_{SDS}	Data Setup Time	200	-	ns
t_{SDH}	Data Hold Time	200	-	ns
t_{CSS}	Chip Select Setup Time	240	-	ns
t_{CSH}	Chip Select Hold Time	120	-	ns
t_{SHW}	Serial Clock H Pulse Width	200	-	ns
t_{SLW}	Serial Clock L Pulse Width	200	-	ns
t_R	Rise Time	-	30	ns
t_F	Fall Time	-	30	ns

(V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25°C)

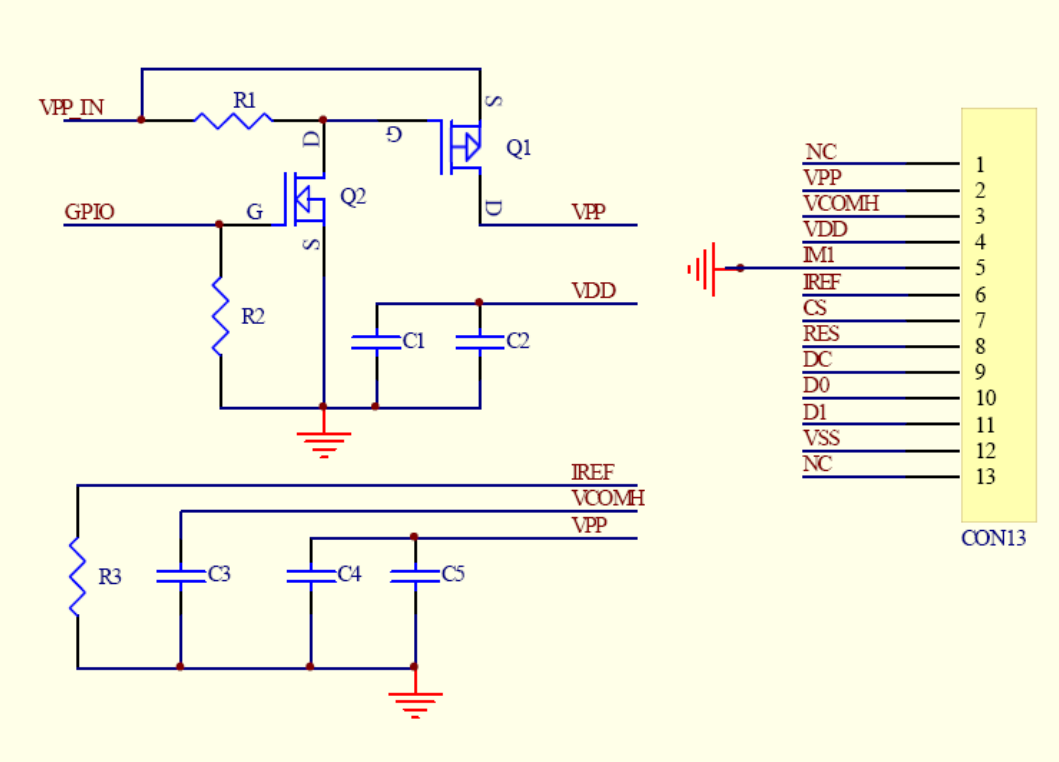
Symbol	Description	Min	Max	Unit
t_{SCYC}	Serial Clock Cycle Time	250	-	ns
t_{SAS}	Address Setup Time	150	-	ns
t_{SAH}	Address Hold Time	150	-	ns
t_{SDS}	Data Setup Time	100	-	ns
t_{SDH}	Data Hold Time	100	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{SHW}	Serial Clock H Pulse Width	100	-	ns
t_{SLW}	Serial Clock L Pulse Width	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns


CS
tCSS
tCSH
tSAS
tSAH
A0
tSCYC
tSLW
SCL
tSHW
tF
tR
tF
tSDS
tSDH
SI

3.3.3.2 4-wire Serial Interface

特别提醒(Special Tips):主板设计务必加电子开关，否则，可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1,:	0.1μF / 6.3V, X5R
C2:	4.7μF / 6.3V, X5R
C3:	2.2μF/ 16V, X7R
C4:	4.7μF / 16V, X7R
C5:	0.1μF / 16V, X7R
R3:	560KΩ, R3 = (Voltage at IREF - VSS) / IREF
R2, R1:	47kΩ
Q1:	FDN338P
Q2:	FDN335N

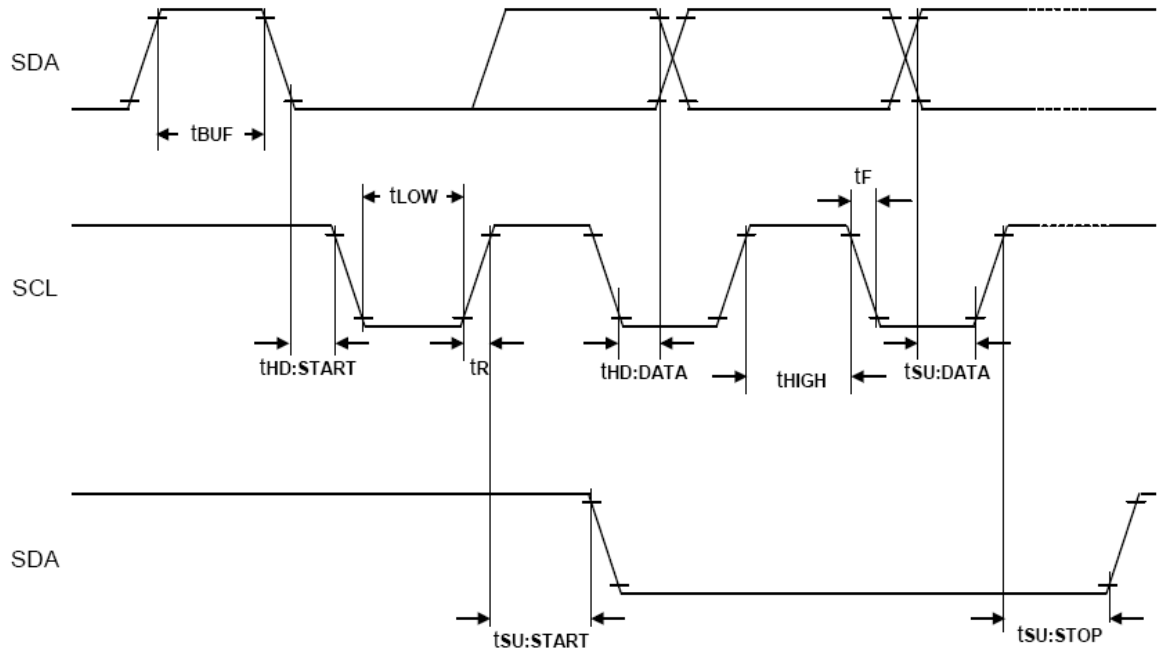
Notes:

VDD:	1.65~3.5V, it should be equal to MPU I/O voltage.
Vpp_in:	8.5~9.5V

3.3.4.1 I2C Interface Timing Characteristics:

(V_{DD} = 1.65 - 3.5V, TA = +25°C)

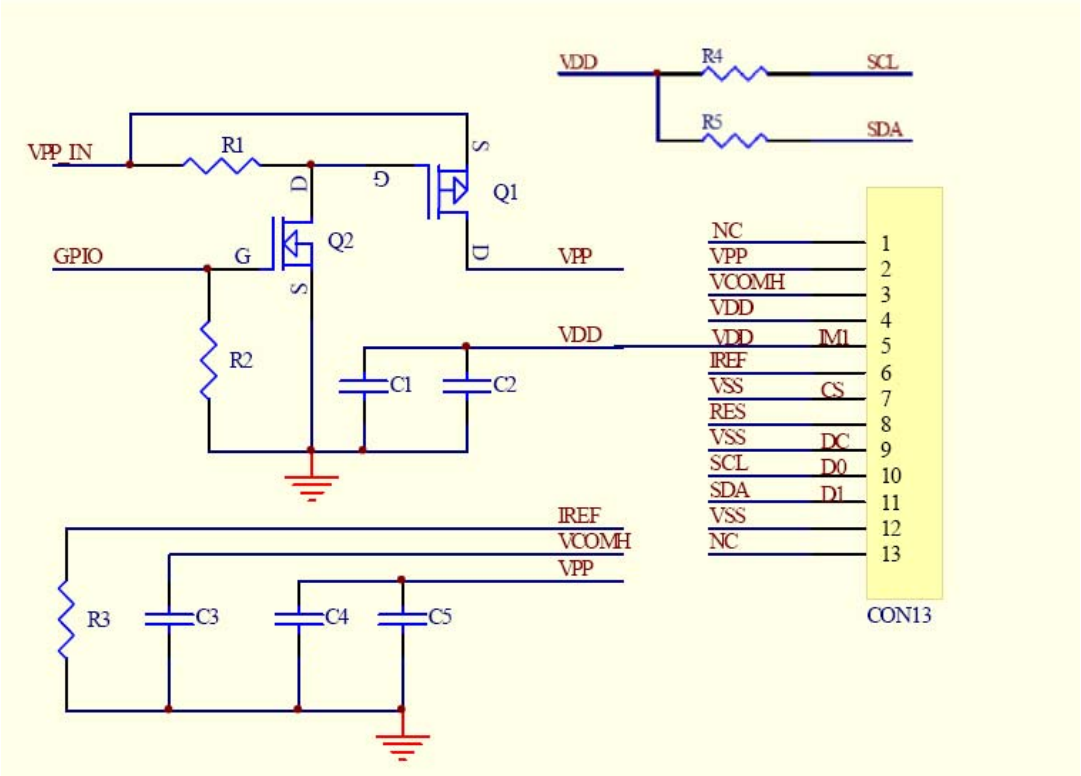
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f_{SCL}	SCL clock frequency	DC	-	400	kHz	
T_{LOW}	SCL clock Low pulse width	1.3	-	-	μs	
T_{HIGH}	SCL clock H pulse width	0.6	-	-	μs	
$T_{SU:DATA}$	data setup time	100	-	-	ns	
$T_{HD:DATA}$	data hold time	0	-	0.9	μs	
T_R	SCL、SDA rise time	20+0.1Cb	-	300	ns	
T_F	SCL、SDA fall time	20+0.1Cb	-	300	ns	
Cb	Capacity load on each bus line	-	-	400	pF	
$T_{SU:START}$	Setup timefor re-START	0.6	-	-	μs	
$T_{HD:START}$	START Hold time	0.6	-	-	μs	
$T_{SU:STOP}$	Setup time for STOP	0.6	-	-	μs	
T_{BUF}	Bus free times between STOP and START condition	1.3	-	-	μs	



3.3.4.2 I²C Interface Characteristics

特别提醒(Special Tips):主板设计务必加电子开关，否则，可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1,:	0.1μF / 6.3V, X5R
C2:	4.7μF / 6.3V, X5R
C3:	4.7μF/ 16V, X7R
C4:	4.7μF / 16V, X7R
C5:	0.1μF / 16V, X7R
R3:	560KΩ, R3 = (Voltage at IREF - VSS) / IREF
R2, R1:	47kΩ
R4, R5 :	4.7 kΩ
Q1:	FDN338P
Q2:	FDN335N

Notes:

VDD:	1.65~3.5V, it should be equal to MPU I/O voltage.
Vpp_in:	8.5~9.5V

4.Functional Specification

4.1 Commands

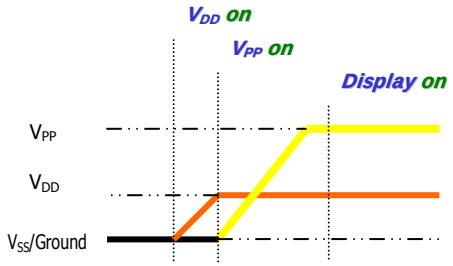
Refer to the Technical Manual for the SH1107

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

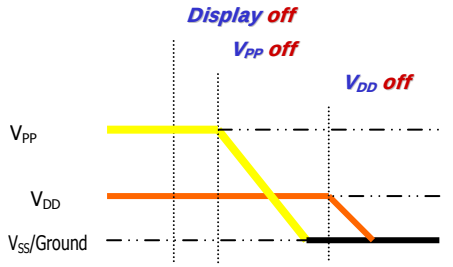
4.2.1 Power up Sequence:

1. Power up VDD
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up VPP
6. Delay 100ms
(When VPP is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down VPP
3. Delay 100ms
(When VPP is reach 0 and panel is completely discharges)
4. Power down VDD



Note 9:

1) Since an ESD protection circuit is connected between VDD and VBPPB inside the driver IC, VPP becomes lower than VDD whenever VBDDB is ON and VPP is OFF.
2) VPPB should be kept float (disable) when it is OFF.
3) Power Pins (VDD, VPP) can never be pulled to ground under any circumstance.
4) VBDDB should not be power down before VPP power down.

4.3 Reset Circuit

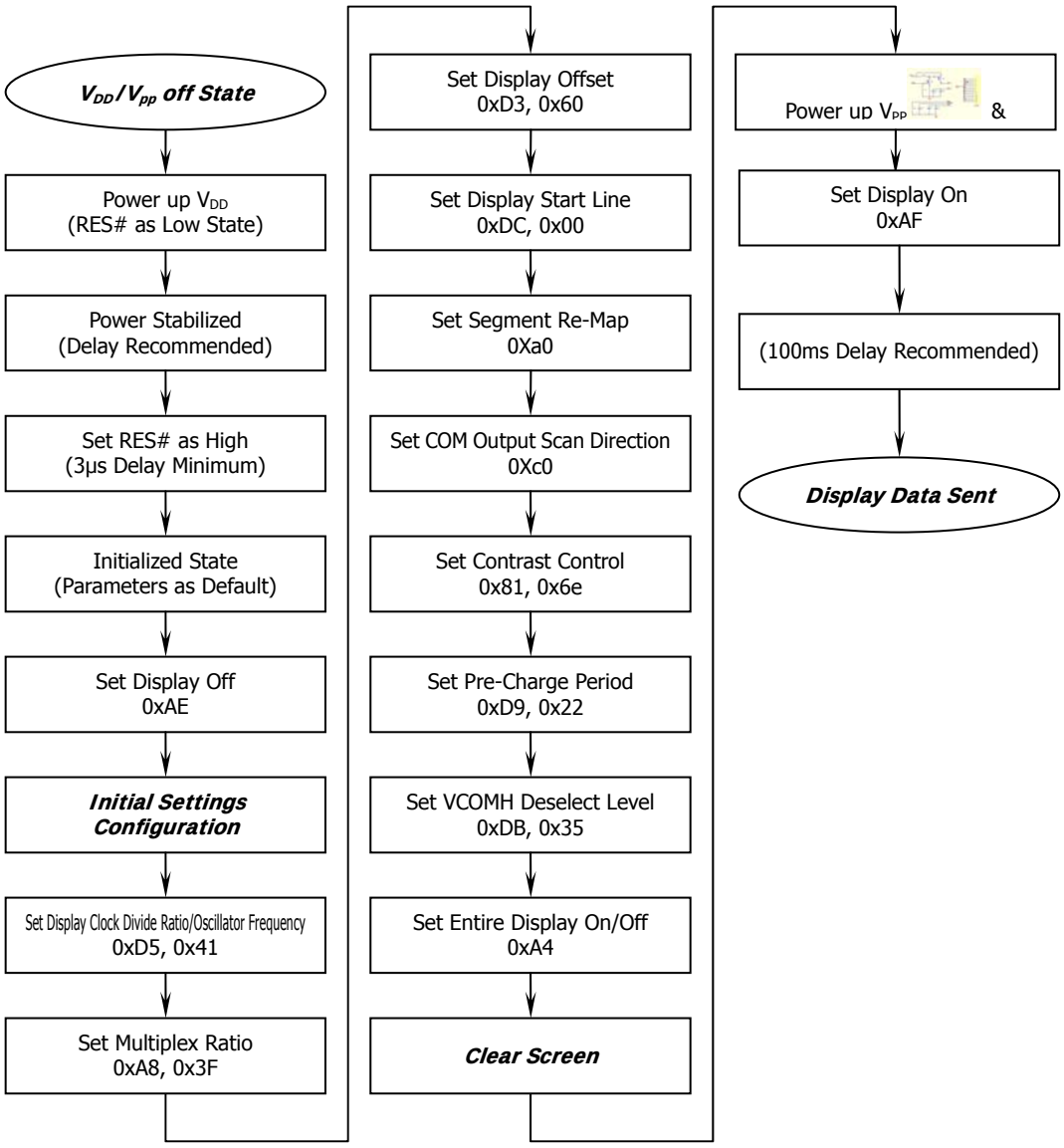
When RESB input is low, the chip is initialized with the following status:

1. Display is OFF. Common and Segment are in high impedance state.
2. 128´128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 is mapped to the top line
of the display).
4. Shift register data clear in serial interface
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control register is set at 80h
8. Internal DC-DC is selected

4.4 Actual Application Example

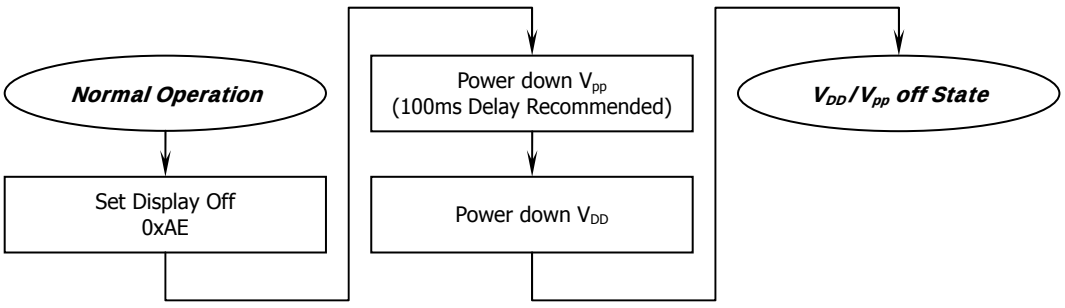
Command usage and explanation of an actual example

4.4.1 V_{pp} Supplied Externally

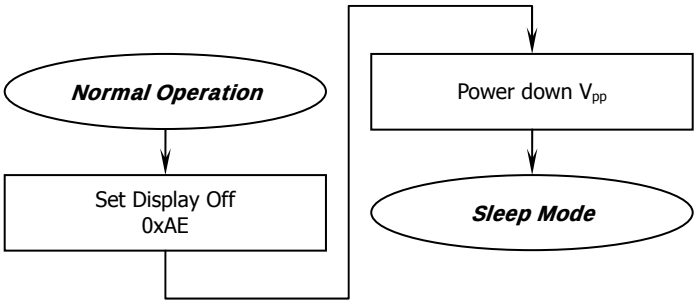


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

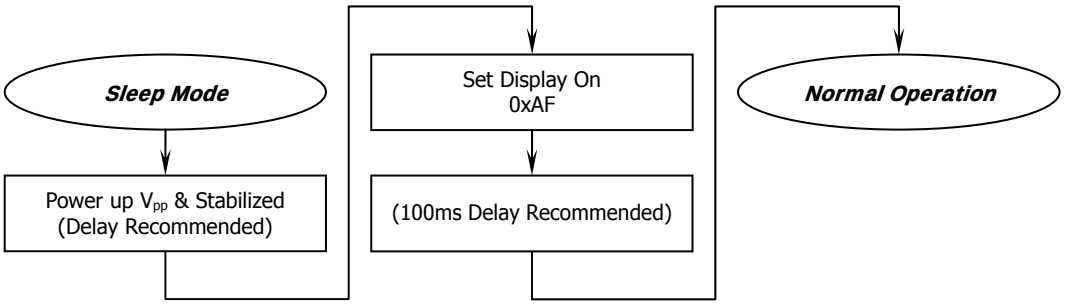
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



External setting
void sh1107()

{

write_i(0xAE); /*display off*/

write_i(0x00); /*set lower column address*/

write_i(0x10); /*set higher column address*/

write_i(0xB0); /*set page address*/

write_i(0xdc); /*set display start line*/

write_i(0x00);

write_i(0x81); /*contract control*/

```
write_i(0x6e);      /*128*/

write_i(0x20);      /* Set Memory addressing mode (0x20/0x21) */

write_i(0xA0);      /*set segment remap*/

write_i(0xC0);      /*Com scan direction*/

write_i(0xA4);      /*Disable Entire Display On (0xA4/0xA5)*/

write_i(0xA6);      /*normal / reverse*/

write_i(0xA8);      /*multiplex ratio*/
write_i(0x3F);      /*duty = 1/64*/

write_i(0xD3);      /*set display offset*/
write_i(0x60);

write_i(0xD5);      /*set osc division*/
write_i(0x41);

write_i(0xD9);      /*set pre-charge period*/
write_i(0x22);
```

```
        write_i(0xdb);      /*set vcomh*/
        write_i(0x35);

        write_i(0xad);      /*set charge pump enable*/
        write_i(0x8a);       /*Set DC-DC enable (a=0:disable; a=1:enable) */

        write_i(0xAF);      /*display ON*/

}
```

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15% RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50cm
Distance between the Panel & Eyes of the Inspector:	≥ 30cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

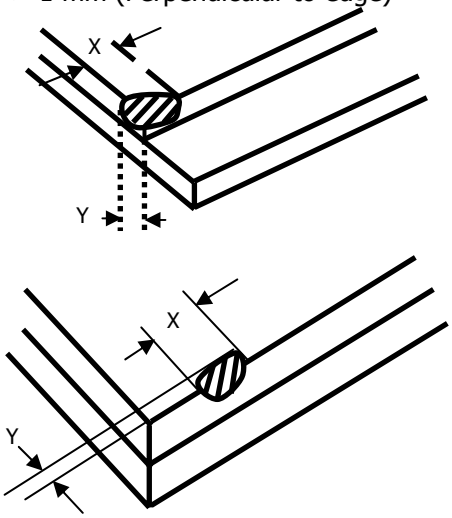
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

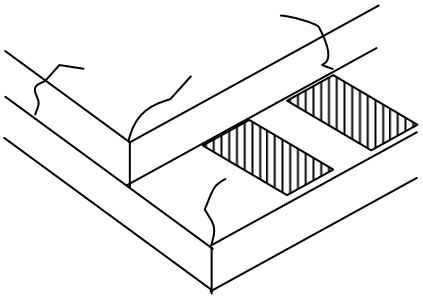
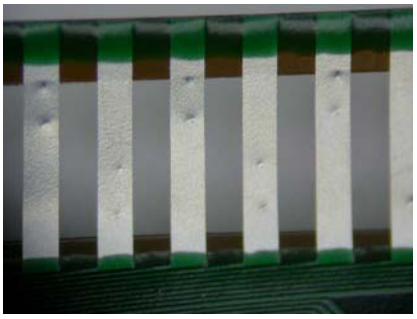
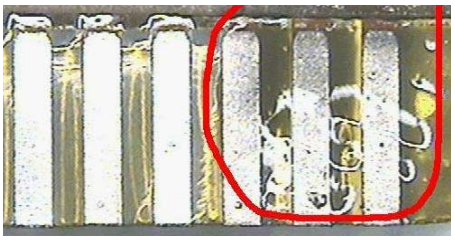
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

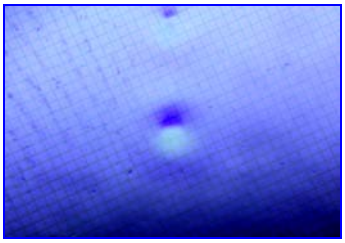
Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

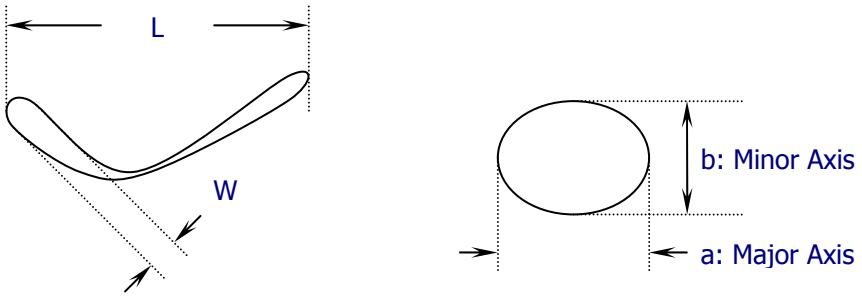
6.3.2 Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

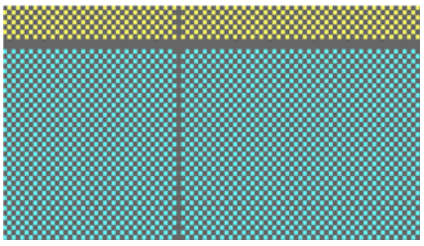
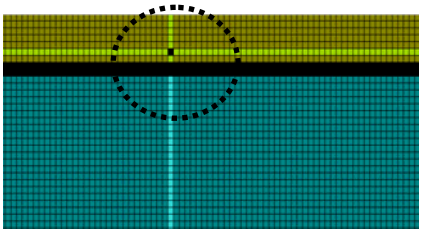
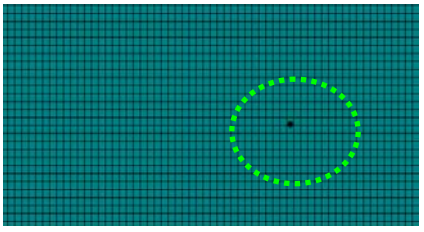
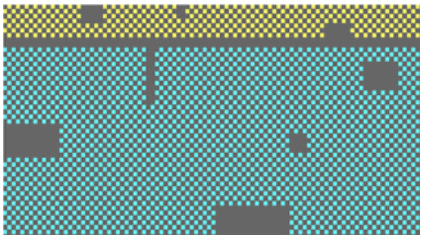
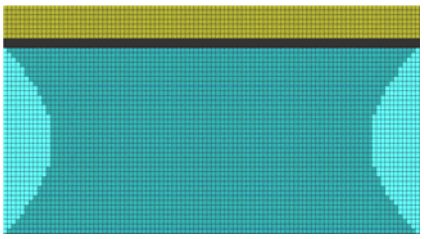
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1 L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.25 n ≤ 1 0.25 < Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

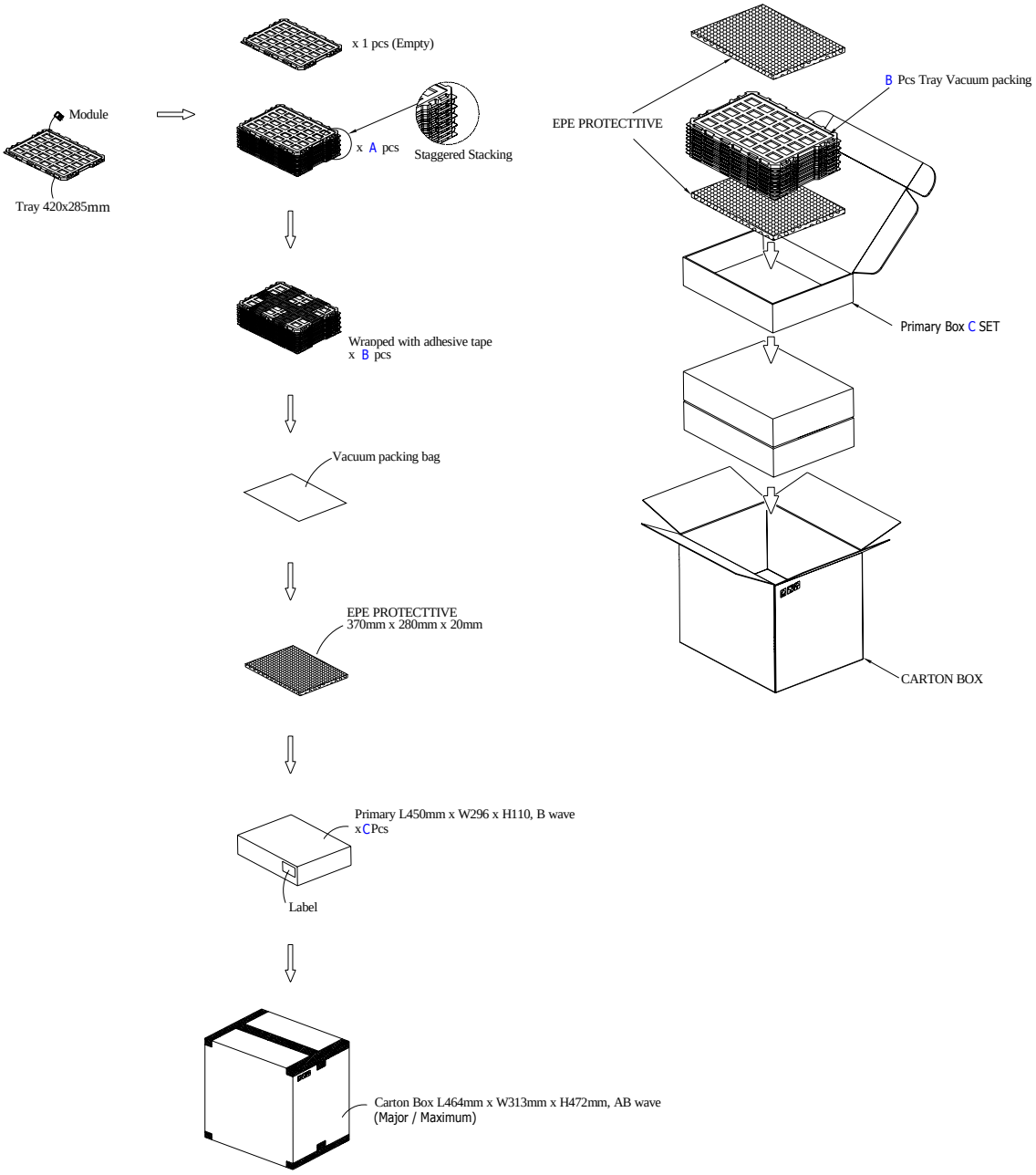
** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2



6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7. Package Specifications



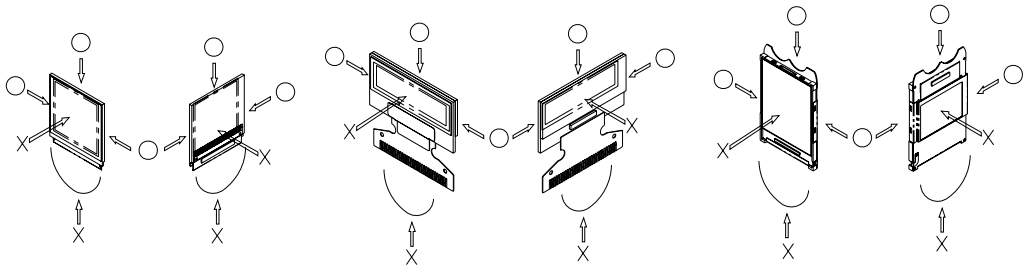
Item		Quantity	
Module		**810**	**per Primary Box**
Holding Trays	**(A)**	**15**	**per Primary Box**
Total Trays	**(B)**	**16**	**per Primary Box (Including 1 Empty Tray)**
Primary Box	**(C)**	**1~4**	**per Carton (4 as Major / Maximum)**

8. Precautions When Using These OEL Display Modules

8.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the driver IC and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Allvision technology Inc.) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the V_{IL} and V_{IH} specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (V_{DD}). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: SH1107
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4 Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5 Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may

be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.

5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.