

MPL3115A2

I2C precision pressure sensor with altimetry

Rev. 5.1 — 13 September 2016 Data sheet: Technical data

1 General description

The MPL3115A2 is a compact, piezoresistive, absolute pressure sensor with an I^2C digital interface. MPL3115A2 has a wide operating range of 20 kPa to 110 kPa, a range that covers all surface elevations on earth. The MEMS is temperature compensated utilizing an on-chip temperature sensor. The pressure and temperature data is fed into a high resolution ADC to provide fully compensated and digitized outputs for pressure in Pascals and temperature in °C. The compensated pressure output can then be converted to altitude, utilizing the formula stated in Section 8.1.3 "Pressure/altitude" provided in meters.The internal processing in MPL3115A2 removes compensation and unit conversion load from the system MCU, simplifying system design.

MPL3115A2's advanced ASIC has multiple user programmable modes such as power saving, interrupt and autonomous data acquisition modes, including programmed acquisition cycle timing, and poll-only modes. Typical active supply current is 40 µA per measurement-second for a stable 10 cm output resolution.

2 Features and benefits

- Operating range: 20 kPa to 110 kPa absolute pressure
- –700 m to be equivalent altitude at 50 kPa
- Calibrated range: 50 kPa to 110 kPa absolute pressure
- Calibrated temperature output: −40 °C to 85 °C
- I^2C digital output interface (up to 400 kHz)
- Fully compensated internally
- Precision ADC resulting in 0.1 meter of effective resolution
- Direct reading
  - Pressure: 20-bit measurement (Pascals)
    - 20 to 110 kPa
  - Altitude: 20-bit measurement (meters)
    - –698 to 11,775 m
  - Temperature: 12-bit measurement (°C)
    - –40 °C to 85 °C
- Programmable interrupts
- Autonomous data acquisition
  - Embedded 32-sample FIFO
  - Data logging up to 12 days using the FIFO
  - One-second to nine-hour data acquisition rate
- 1.95 V to 3.6 V supply voltage, internally regulated
- 1.6 V to 3.6 V digital interface supply voltage
- Operating temperature from −40 °C to +85 °C

3 Applications

- High-accuracy altimetry and barometry
- Smartphones, tablets and wearable devices
- GPS applications: dead reckoning, map assist, navigation, enhancement for emergency services
- Weather station equipment

4 Ordering information

Table 1. Ordering information

Device number	Shipping	Package	Number of ports			Pressure Type			Digital interface
			None	Single	Dual	Gauge	Differential	Absolute	
MPL3115A2	Tray	98ASA002260D	•	—	—	—	—	•	•
MPL3115A2R1	Tape and reel	98ASA002260D	•	—	—	—	—	•	•

5 Block diagram

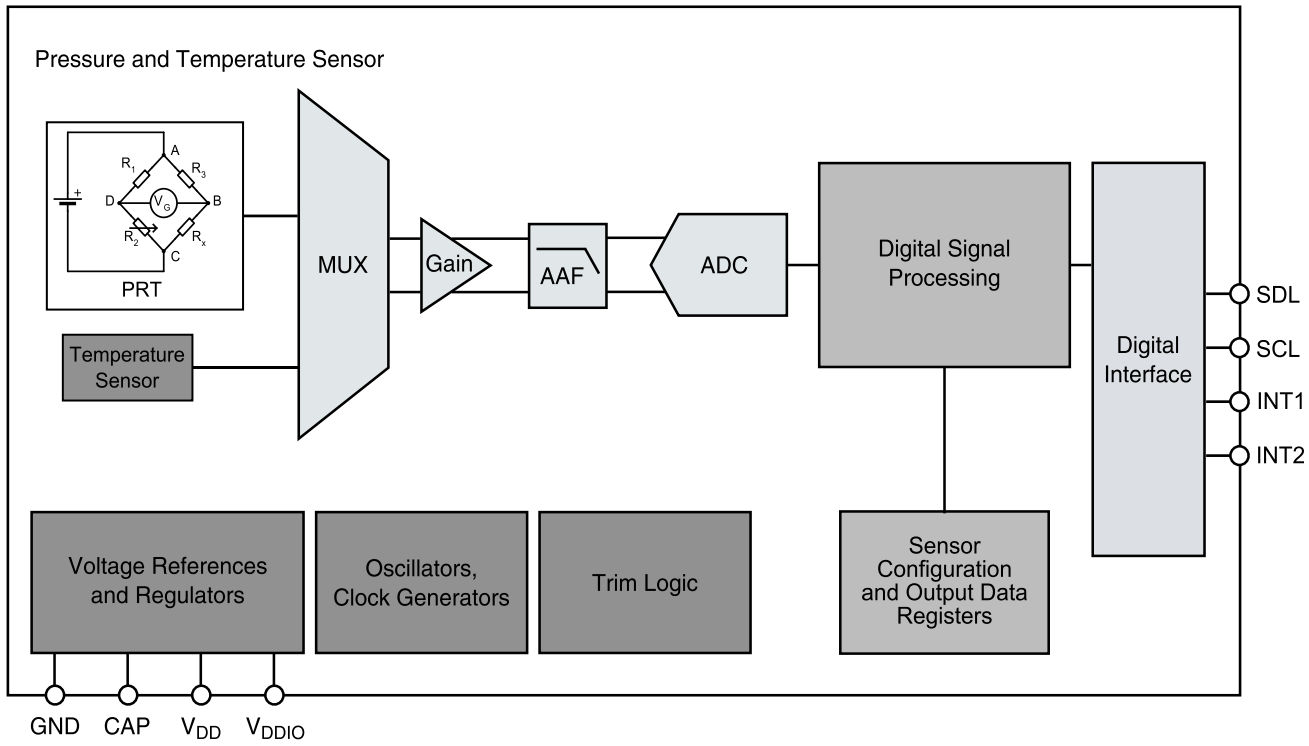


Figure 1. Block diagram

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

6 Pinning information

6.1 Pinning

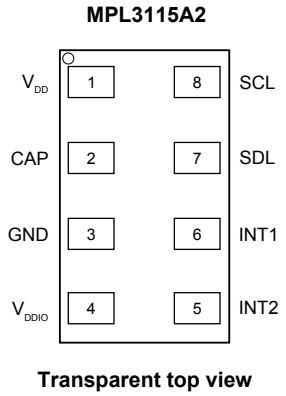


Figure 2. 8-pin LGA pinout

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{DD}	1	V_{DD} power supply connection (1.95 to 3.6 V)
CAP	2	External capacitor
GND	3	Ground
V_{DDIO}	4	Digital interface power supply (1.62 to 3.6 V)
INT2	5	Pressure interrupt 2
INT1	6	Pressure interrupt 1
SDL	7	I^2C serial data
SCL	8	I^2C serial clock

7 System connections

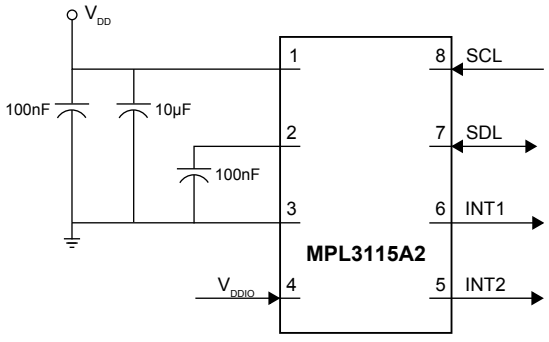


Figure 3. Typical application diagram

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

The device power is supplied through the V_{DD} line. Power supply decoupling capacitors (100 nF ceramic plus 10 µF bulk or 10 µF ceramic) should be placed as near as possible to pin 1 of the device. A second 100 nF capacitor is used to bypass the internal regulator. The functions, threshold and the timing of the interrupt pins (INT1 and INT2) are user programmable through the I^2C interface.

8 Mechanical and electrical specifications

8.1 Terminology

8.1.1 Resolution

The resolution of a pressure sensor is the minimum change of pressure that can be reliably measured. The usable resolution of the device is programmable, enabling the user to choose a compromise between acquisition speed, power consumption, and resolution that best fits the application. To simplify the programming, the data is always reported in the same format with differing number of usable bits.

8.1.2 Accuracy

8.1.2.1 Offset

The offset is defined as the output signal obtained when the reference pressure (a vacuum for an absolute pressure sensor) is applied to the sensor. Offset error affects absolute pressure measurements but not relative pressure measurements. An altitude measurement is the pressure value in comparison to sea level, a barometric measurement is the pressure value read by the sensor. That is, a measurement of total pressure seen (for example 70 kPa), or total height (for example 3000 m) above sea level. A change in the offset will affect the pressure value or height seen above sea level as it shifts the sea level base reference. An absolute pressure measurement is not the same as relative pressure measurement, where the pressure is compared when raising or lowering pressure in shorter intervals. This would be a walk up a hill, measuring the pressure and altitude difference from start to finish. In the relative case, the offset shifts are shared in the two absolute measurements and negate each other during the pressure calculation.

For the MPL3115A2, the long term offset shift can be removed by adjusting the pressure or altitude offset correction. See Section 13.23 "Offset correction registers".This adjustment is provided to override the factory programmed values to compensate for offsets introduced by manufacturing and mounting stresses. It is highly recommended that this is utilized to realize the full accuracy potential of the device.

8.1.2.2 Linearity

Linearity compares the slope of the measurement data to that of an ideal transfer function. It refers to how well a transducer's output follows the equation $P_{OUT} = P_{OFF}$ + sensitivity × P straight-line equation over the operating pressure range. The method used by NXP to give the linearity specification is the end-point straight line method measured at midrange pressure.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

8.1.2.3 Absolute pressure

Absolute pressure sensors measure an external pressure relative to a zero-pressure reference (vacuum) sealed inside the reference chamber of the die during manufacturing. This standard allows comparison to a standard value set such that 14.7 psi = 101,325 Pa = 1 atm at sea level as a measurement target. The absolute pressure is used to determine altitude as it has a constant reference for comparison. Measurement at sea level can be compared to measurement at a mountain summit as they use the same vacuum reference. The conversion of absolute pressure to altitude in meters is calculated based on US Standard Atmosphere 1976 (NASA).

Note: *Absolute pressure is not linear in relation to altitude, it is an exponential function. The value of altitude can be read directly from the device in increments of 0.0625 meters, or the value of pressure in 0.25 Pascal (Pa) units.*

8.1.2.4 Span

Span is the value of full-scale output with offset subtracted, representing the full range of the pressure sensor. Ideally the span is a specification over a constant temperature. The device uses internal temperature compensation to remove drift. Span accuracy is the comparison of the measured difference and the actual difference between the highest and lowest pressures in the specified range.

8.1.3 Pressure/altitude

The device is a high accuracy pressure sensor with integrated data calculation and logging capabilities. To provide altitude readings, the altitude calculations are based on the measured pressure (p), the user input of the equivalent sea level pressure to compensate for local weather conditions (OFF_H) and the US Standard Atmosphere 1976 (NASA). Pressure is given in Pascals (Pa), and fractions of a Pa. Altitude is given in meters (m) and fractions of a meter. The altitude is calculated from the pressure using the following equation:

$$h = 44330.77\left\{1 - \left(\frac{p}{p_0}\right)^{0.1902632}\right\} + OFF_H\ (Register\ value)$$

where:

p_0 = sea level pressure (101,326 Pa)
h = altitude in meters

8.2 Absolute maximum ratings

Absolute maximum ratings are the limits the device can be exposed to without permanently damaging it. Absolute maximum ratings are stress ratings only, functional operation at these ratings is not guaranteed. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

This device contains circuitry to protect against damage due to high static voltage or electrical fields. It is advised, however, that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Table 3. Maximum ratings

Symbol	Characteristic	Value	Unit
P_{max}	Maximum applied pressure	500	kPa
V_{DD}	Supply voltage	−0.3 to 3.6	V
V_{DDIO}	Interface supply voltage	−0.3 to 3.6	V
V_{IN}	Input voltage on any control pin (SCL, SDA)	−0.3 to V_{DDIO} + 0.3	V
T_{OP}	Operating temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−40 to +125	°C

Table 4. ESD and latchup protection characteristics

Symbol	Rating	Value	Unit
HBM	Human body model	±2000	V
CDM	Charge device model	±500	V
—	Latchup current at T = 85 °C	±100	mA



Caution

This device is sensitive to mechanical shock. Improper handling can cause permanent damage to the part or cause the part to otherwise fail.



msc896

Caution

This is an ESD sensitive device. Improper handling can cause permanent damage to the part.

8.3 Mechanical characteristics

Table 5. Mechanical characteristics

V_{DD} = 2.5 V, T = 25 °C, over 50 kPa to 110 kPa, unless otherwise noted.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Pressure sensor						
P_{FS}	Measurement range	Calibrated range	50	—	110	kPa
		Operational range	20	—	110	kPa
	Pressure reading noise [1]	1x oversample	—	19	—	Pa RMS
		128x oversample	—	1.5	—	Pa RMS
	Pressure absolute accuracy	50 to 110 kPa over 0 °C to 50 °C	–0.4	—	0.4	kPa
		50 to 110 kPa over−10 °C to 70 °C	—	±0.4	—	kPa

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
	Pressure relative accuracy	Relative accuracy during pressure change between 70 to 110 kPa at any constant temperature between −10 °C to 50 °C	—	±0.05	—	kPa
		Relative accuracy during changing temperature between −10 °C to 50 °C at any constant pressure between 50 kPa to 110 kPa	—	±0.1	—	kPa
	Pressure/altitude resolution [2][3][4]	Barometer mode	0.25	1.5	—	Pa
		Altimeter mode	0.0625	0.3	—	m
	Output data rate	One-shot mode	—	100	—	Hz
		FIFO mode	—	—	1	Hz
	Board mount drift	After solder reflow	—	±0.15	—	kPa
	Long term drift	After a period of 1 year	—	±0.1	—	kPa
Temperature sensor						
T_{FS}	Measurement range	—	–40	—	+85	°C
	Temperature accuracy	@25 °C	—	±1	—	°C
		Over temperature range	—	±3	—	°C
T_{OP}	Operating temperature range	—	–40	—	+85	°C

[1] Oversample (OSR) modes internally combine and average samples to reduce noise.
[2] Smallest bit change in register represents minimum value change in Pascals or meters. Typical resolution to signify change in altitude is 0.3 m.
[3] Reference pressure = 101.325 kPa (sea level).
[4] At 128x oversample ratio.

8.4 Electrical characteristics

Table 6. Electrical characteristics

@ V_{DD} = 2.5 V, T = 25 °C unless otherwise noted.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DDIO}	I/O supply voltage	—	1.62	1.8	3.6	V
V_{DD}	Operating supply voltage	—	1.95	2.5	3.6	V
I_{DD}	Integrated current 1 update per second	Highest speed mode oversample = 1	—	8.5	—	µA
		Standard mode oversample = 16	—	40	—	µA
		High resolution mode oversample = 128	—	265	—	µA
I_{DDMAX}	Max current during acquisition and conversion	During acquisition/ conversion	—	2	—	mA
I_{DDSTBY}	Supply current drain in STANDBY mode	STANDBY mode selected SBYB = 0	—	2	—	µA

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
VIH	Digital high level input voltage SCL, SDA	—	0.75	—	—	V_{DDIO}
VIL	Digital low level input voltage SCL, SDA	—	—	—	0.3	V_{DDIO}
VOH	High level output voltage INT1, INT2	I_O = 500 µA	0.9	—	—	V_{DDIO}
VOL	Low level output voltage INT1, INT2	I_O = 500 µA	—	—	0.1	V_{DDIO}
VOLS	Low level output voltage SDA	I_O = 500 µA	—	—	0.1	V_{DDIO}
T_{ON}	Turn-on time [1][2][3]	High speed mode	—	—	60	ms
		High resolution mode	—	—	1000	ms
T_{OP}	Operating temperature range	—	−40	25	+85	°C
I^2C addressing						
I^2C Address	—	—		0x60		Hex
The device uses 7-bit addressing and does not acknowledge general call address 000 0000. Slave address has been set to 60h or 110 0000. 8-bit read is C1h, 8-bit write is C0h.						

[1] Time to obtain valid data from STANDBY mode to ACTIVE mode
[2] High speed mode is achieved by setting the oversample rate of 1x.
[3] High resolution mode is achieved by setting the oversample to 128x.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

9 Digital interface

The registers embedded inside the device are accessed through an I^2C serial interface.

Table 7. Serial interface pin descriptions

Name	Description
SCL	I^2C serial clock
SDA	I^2C serial data

9.1 I^2C characteristics

Table 8. I^2C Slave timing values

All values referred to VIH(min) and VIL(max) levels.

Symbol	Parameter	I^2C			Unit
		Condition	Min	Max	
f_{SCL}	SCL clock frequency	Pull-up = 1 kΩ, Cb = 400 pF	0	400	kHz
f_{SCL}	SCL clock frequency	Pull-up = 1 kΩ, Cb = 20 pF	0	4	MHz
t_{BUF}	Bus free time between STOP and START condition	—	1.3	—	µs
$t_{HD;STA}$	Repeated START hold time	—	0.6	—	µs
$t_{SU;STA}$	Repeated START setup time	—	0.6	—	µs
$t_{SU;STO}$	STOP condition setup time	—	0.6	—	µs
$t_{HD;DAT}$	SDA data hold time [1][2][3]	—	50	—	ns
$t_{SU;DAT}$	SDA setup time [4]	—	100	—	ns
t_{LOW}	SCL clock low time	—	1.3	—	µs
t_{HIGH}	SCL clock high time	—	0.6	—	µs
t_r	SDA and SCL rise time [5]	—	$20 + 0.1C_b$	300	ns
t_f	SDA and SCL fall Time [2][5][6][7]	—	$20+ 0.1C_b$	300	ns
t_{SP}	Pulse width of spikes that are suppressed by internal input filter	—	—	50	ns

[1] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.

[2] The device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the VIH(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL

[3] The maximum $t_{HD;DAT}$ must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This device does not stretch the LOW period (t_{LOW}) of the SCL signal.

[4] A fast mode I^2C device can be used in a standard mode I^2C system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_r(max) + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the standard mode I^2C specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

[5] Cb = Total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In fast mode plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

9.2 I²C operation

The transaction on the bus is started through a start condition (START) signal. START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After START has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after START contains the slave address in the first 7 bits, and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master. The ninth clock pulse, following the slave address byte (and each subsequent byte) is the acknowledge (ACK).The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock period.

The number of bytes per transfer is unlimited. If the master cannot receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL low to force the transmitter into a wait state. Data transfer only continues when the master is ready for another byte and releases the clock line.

A low to high transition on the SDA line while the SCL line is high is defined as a stop condition (STOP). A data transfer is always terminated by a STOP. A master may also issue a repeated START during a data transfer. Device expects repeated STARTs to be used to randomly read from specific registers.

The standard 7-bit I²C slave address is 60h or 1100000. 8-bit read is C1h, 8-bit write is C0h.

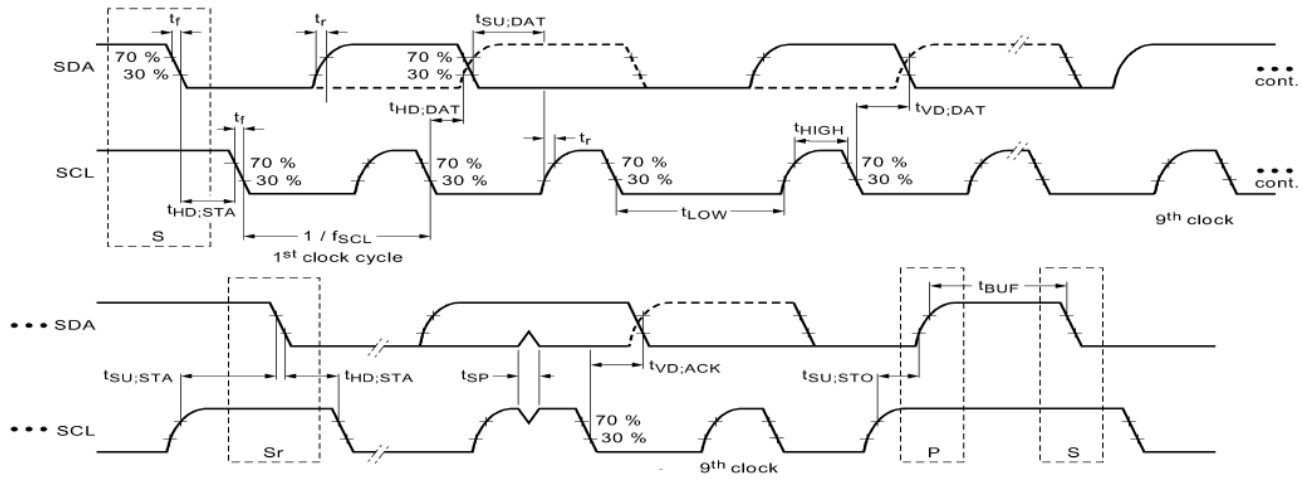


Figure 4. I²C slave timing diagram

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

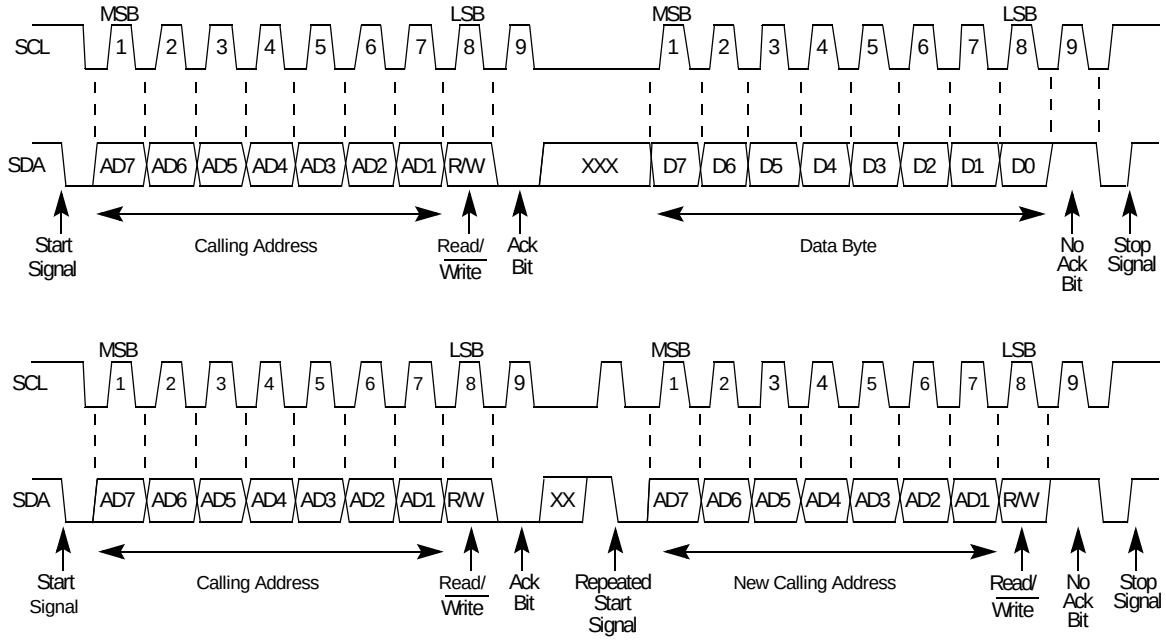


Figure 5. I²C bus transmission signals

Consult factory for alternate addresses. See the application note titled Sensor I²C Setup and FAQ (document AN4481).

10 Modes of operation

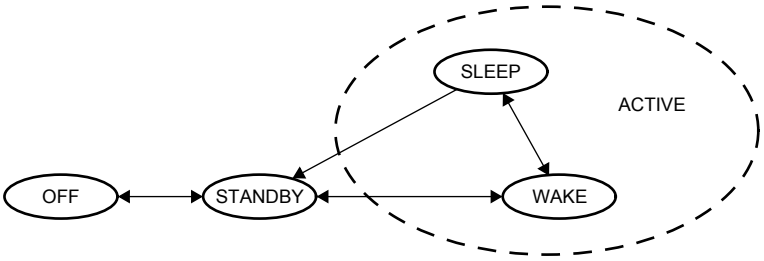


Figure 6. Mode transition diagram

Table 9. Mode of operation description

Mode	I²C-bus state	V_{DD}	Condition	Function description
OFF	Powered down	< 1.62 V	< V_{DD} + 0.3 V	Device is powered off.
STANDBY	I²C/SPI communication with the device is possible	ON	SBYB bit of CTRL_REG1 is cleared	Only POR and digital blocks are enabled. Analog subsystem is disabled.
ACTIVE	I²C/SPI communication with the device is possible	ON	SBYB bit of CTRL_REG1 is set	All blocks are enabled (POR, digital, analog).

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

10.1 OFF

Unit is powered down and has no operating functionality. V_{DD} and V_{DDIO} are not powered.

10.2 STANDBY

The digital sections are operational and the unit is capable of receiving commands and delivering stored data. The analog sections are off. The part is waiting for CTRL_REG1 to be configured and the part to enter active mode.

10.3 ACTIVE

Both analog and digital sections are running. The unit is capable of gathering new data, and accepting commands. The device is fully functional.

11 Quick start setup

To set up the device in altimeter mode, you may select your data retrieval method between polling (no FIFO), interrupt (no FIFO) or with the FIFO. The flow charts in Figure 7 and Figure 8 describe the setup for polling or interrupt with an OSR of 128.

For more information, see application note titled Data Manipulation and Basic Settings of the MPL3115A2 Command Line Interface (document AN4519).

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

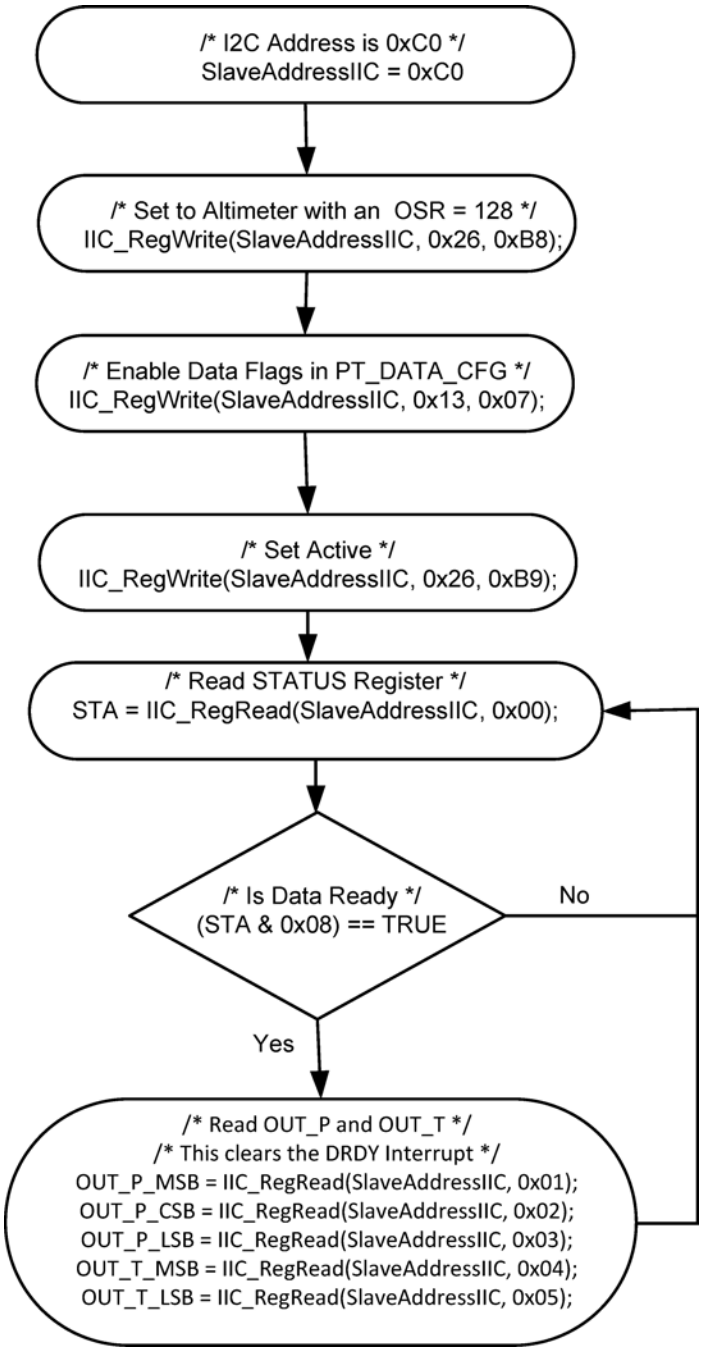


Figure 7. Polling - no FIFO

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

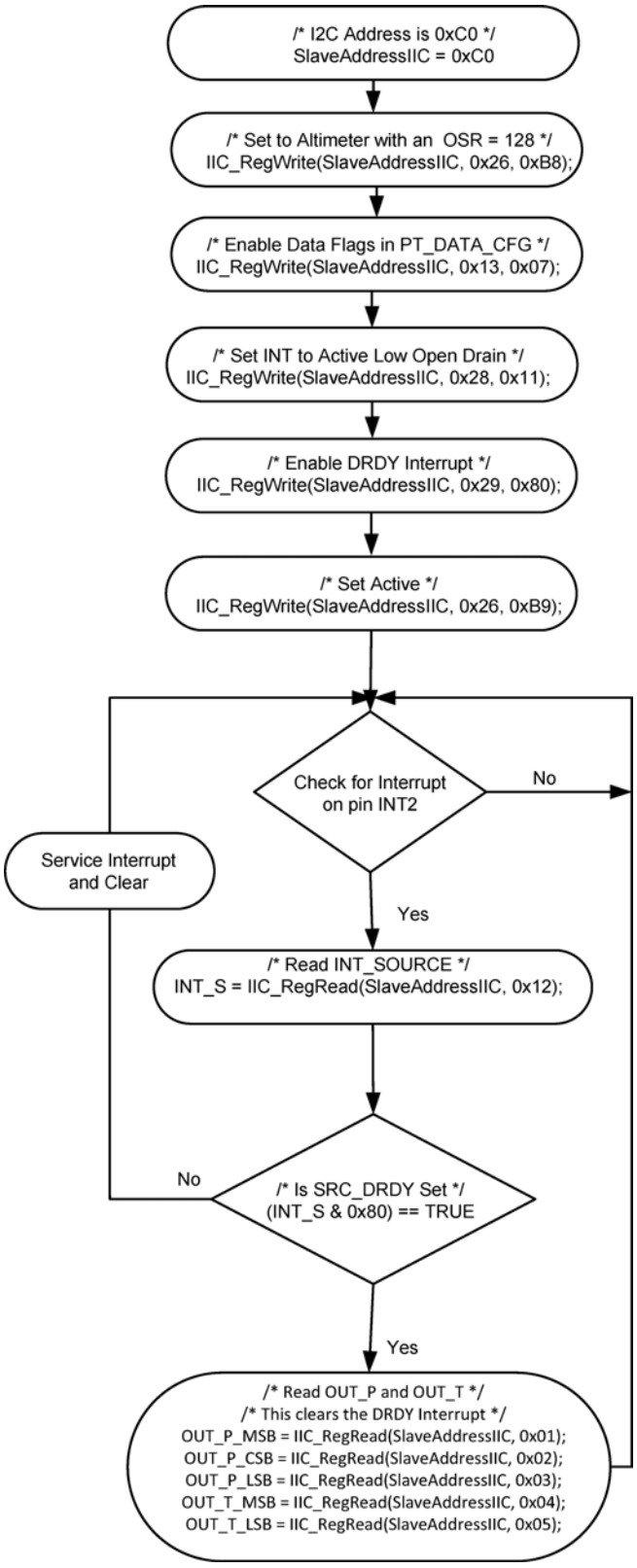


Figure 8. Interrupt - no FIFO

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

12 Functionality

The device is a low-power, high accuracy, digital output altimeter, barometer and thermometer, packaged in a 3 x 5 x 1.1 mm form factor. The complete device includes a sensing element, analog and digital signal processing and an I^2C interface.

The device has two operational modes, barometer and altimeter. Both modes include a thermometer temperature output function.

Power consumption and sensitivity are programmable where the data oversampling ratio can be set to balance current consumption and noise/resolution. Serial interface communication is through an I^2C interface thus making the device particularly suitable for direct interfacing with a microcontroller. The device features two independently programmable interrupt signals INT1 and INT2. These can be set to generate an interrupt signal when a new set of pressure/altitude and temperature data is available, thereby simplifying data acquisition for the host controller. These interrupt pins can also be configured to generate interrupts when a user programmed set of conditions are met (see Section 12.6 "External interrupts").

Examples are:

- interrupt can be triggered when a single new data acquisition is ready
- when a desired number of samples are stored within the internal FIFO
- when a change of pressure/altitude or temperature is detected.

In RAW mode, the FIFO must be disabled and all other functionality including alarms, deltas and other interrupts are disabled.

12.1 Factory calibration

The device is factory calibrated for sensitivity, offset for both temperature and pressure measurements. Trim values are stored on-chip, in non-volatile memory (NVM). In normal use, further calibration is not necessary. However, in order to realize the highest possible accuracy, the device allows the user to override the factory set offset values after power-up. The user adjustments are stored in volatile registers. The factory calibration values are not affected, and are always used by default on power-up.

12.2 Barometer/altimeter function

The mode of operation of the device can be selected as barometer or altimeter. The internal sensor gives an absolute pressure signal. The absolute pressure signal is processed to provide a scaled pressure or an altitude, depending on the mode selected. The combination of a high performance sensor and the signal processing enable resolution of pressures below 1 Pa and altitude resolution of better than 1 m at sea level.

When in barometer mode, all pressure related data is reported as 20-bit unsigned data in Pascals. When in altimeter mode, all pressure data is converted to equivalent altitude, based on the US standard atmosphere and then stored as 20-bit 2's complement value in meters and fractions of a meter.

12.2.1 Barometric input

In order to accurately determine the altitude by pressure, the OFF_H register (see Section 13.23.3 "OFF_H - altitude data user offset register (address 2Dh)") is provided to

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

input the local barometric pressure correction. The default value is 101,326 Pa since the BAR_IN_MSB and BAR_IN_LSB registers are in units of 2 Pascals per LSB.

12.3 Temperature function

The unit contains a high-resolution temperature sensor that provides data to the user via a 16-bit data register, as well as for internal compensation of the pressure sensor.

12.4 Autonomous data acquisition

The unit can be programmed to periodically capture altitude/pressure and temperature data. Up to 32 data acquisitions can be stored in the internal FIFO. The interval between acquisitions is programmable from one second to nine hours.

Data collection capabilities: (up to 32 samples over 12 days). The unit can also be programmed to make a single reading and then go to standby mode.

12.5 FIFO

A 32-sample FIFO is incorporated to minimize the overhead of collecting multiple data samples. The FIFO stores both temperature and pressure/altitude data. The device can be programmed to autonomously collect data at programmed intervals and store the data in the FIFO. FIFO interrupts can be triggered by watermark full or data contention (FIFO GATE) events.

12.6 External interrupts

Two independent interrupt out pins are provided. The configuration of the pins are programmable (polarity, open drain or push/pull.) Any one of the internal interrupt sources can be routed to either pin.

12.6.1 Reach target threshold pressure/altitude (SRC_PTH)

The interrupt flag is set on reaching the value stored in the pressure/altitude target register. Additionally, a window value provides the ability to signal when the target is nearing the value in the pressure/altitude target register from either above or below. When in barometer mode, these values represent pressures rather than altitudes.

Examples:

- Set altitude alert to 3000 m and window value to 100 m, interrupt is asserted passing 2900 m, 3000 m, and 3100 m.
- Set pressure alert to 100.0 kPa and window value to 5 kPa, interrupt can be sent passing 95 kPa, 100 kPa, and 105 kPa.

Note: *When the window value is set to 0 then the interrupt will only be generated when reaching or crossing the target value.*

12.6.2 Reach window target pressure/altitude (SRC_PW)

The interrupt flag is set when the pressure/altitude value is within the window defined by the following formula:

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

$$Window = P_TGT_{MSB,LSB} + P_WIND_{MSB,LSB}$$

Note: *No interrupt is generated if the P_WND value is set to 0.*

12.6.3 Reach target threshold temperature (SRC_TTH)

Interrupt flag is set on reaching the value stored in the temperature target register. Additionally a window value provides ability to signal when the target is nearing from either above or below the value in the temperature target register.

Note: *When the window value is set to 0 then the interrupt will only be generated when reaching or crossing the target value.*

12.6.4 Reach window target temperature (SRC_TW)

The interrupt flag is set when the temperature value is within the window defined by the following formula:

$$Window = T_TGT \pm T_WIND$$

Note: *No interrupt is generated if the T_WND value is set to 0.*

12.6.5 Pressure/altitude change (SRC_PCHG)

Interrupt flag is set if sequential pressure/altitude acquisitions exceed value stored in pressure/altitude window value register.

12.6.6 Temperature change (SRC_TCHG)

Interrupt flag is set if sequential temperature acquisitions exceed the value stored in pressure/altitude window value register.

12.6.7 Data ready

Interrupt flag is set when new data or a data overwrite event has occurred. PTOW and/or PTDR (DR_STATUS register) must be set for an interrupt to be generated.

12.6.8 FIFO event

Interrupt flag is set when either an overflow or watermark event has occurred. For more information see Section 13.8 "FIFO setup registers".

12.6.9 Pressure/altitude and temperature delta

Registers show the differences from the last pressure/altitude and temperature samples.

12.6.10 Min/max data value storage

Registers record the minimum and maximum pressure/altitude and temperature.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

13 Register descriptions

Table 10. Register address map

Register Address	Name	Access	Reset value	Description	Reset when STBY to Active	Comment	Auto-increment address	Reference
00h	STATUS	R	00h	Sensor status register [1][2]	Yes	Alias for DR_STATUS or F_STATUS	01h	Section 13.1
01h	OUT_P_MSB	R	00h	Pressure data out MSB [1][2]	Yes	Bits 12 to 19 of 20-bit real-time pressure sample. Root pointer to pressure and temperature FIFO data.	02h 01h	Section 13.3
02h	OUT_P_CSB	R	00h	Pressure data out CSB [1][2]	Yes	Bits 4 to 11 of 20-bit real-time pressure sample	03h	Section 13.3
03h	OUT_P_LSB	R	00h	Pressure data out LSB [1][2]	Yes	Bits 0 to 3 of 20-bit real-time pressure sample	04h	Section 13.3
04h	OUT_T_MSB	R	00h	Temperature data out MSB [1][2]	Yes	Bits 4 to 11 of 12-bit real-time temperature sample	05h	Section 13.4
05h	OUT_T_LSB	R	00h	Temperature data out LSB [1][2]	Yes	Bits 0 to 3 of 12-bit real-time temperature sample	00h	Section 13.4
06h/00h	DR_STATUS	R	00h	Sensor status register [1][2]	Yes	Data ready status information	07h	Section 13.2
07h	OUT_P_DELTA_MSB	R	00h	Pressure data out delta MSB [1][2]	Yes	Bits 12 to 19 of 20-bit pressure change data	08h	Section 13.5
08h	OUT_P_DELTA_CSB	R	00h	Pressure data out delta CSB [1][2]	Yes	Bits 4 to 11 of 20-bit pressure change data	09h	Section 13.5
09h	OUT_P_DELTA_LSB	R	00h	Pressure data out delta LSB [1][2]	Yes	Bits 0 to 3 of 20-bit pressure change data	0Ah	Section 13.5
0Ah	OUT_T_DELTA_MSB	R	00h	Temperature data out delta MSB [1][2]	Yes	Bits 4 to 11 of 12-bit temperature change data	0Bh	Section 13.6
0Bh	OUT_T_DELTA_LSB	R	00h	Temperature data out delta LSB [1][2]	Yes	Bits 0 to 3 of 12-bit temperature change data	06h	Section 13.6
0Ch	WHO_AM_I	R	C4h	Device identification register	No	Fixed device ID number	0Dh	Section 13.7
0Dh	F_STATUS	R	00h	FIFO status register [1][2]	Yes	FIFO status: no FIFO event detected	0Eh	Section 13.8.1
0Eh/01h	F_DATA	R	00h	FIFO 8-bit data access [1][2]	Yes	FIFO 8-bit data access	0Eh	Section 13.8.2
0Fh	F_SETUP	R/W	00h	FIFO setup register [1][3]	No	FIFO setup	10h	Section 13.8.3
10h	TIME_DLY	R	00h	Time delay register [1][2]	Yes	Time since FIFO overflow	11h	Section 13.9
11h	SYSMOD	R	00h	System mode register [2]	Yes	Current system mode	12h	Section 13.10
12h	INT_SOURCE	R	00h	Interrupt source register [1]	No	Interrupt status	13h	Section 13.11
13h	PT_DATA_CFG	R/W	00h	PT data configuration register [1][3]	No	Data event flag configuration	14h	Section 13.12
14h	BAR_IN_MSB	R/W	C5h	BAR input in MSB [1][3]	No	Barometric input for altitude calculation bits 8 to15	15h	Section 13.13
15h	BAR_IN_LSB	R/W	E7h	BAR input in LSB [1][3]	No	Barometric input for altitude calculation bits 0 to 7	16h	Section 13.13
16h	P_TGT_MSB	R/W	00h	Pressure target MSB [1][3]	No	Pressure/altitude target value bits 8 to 15	17h	Section 13.14
17h	P_TGT_LSB	R/W	00h	Pressure target LSB [1][3]	No	Pressure/altitude target value bits 0 to 7	18h	Section 13.14
18h	T_TGT	R/W	00h	Temperature target register [1][3]	No	Temperature target value	19h	Section 13.15
19h	P_WND_MSB	R/W	00h	Pressure/altitude window MSB [1][3]	No	Pressure/altitude window value bits 8 to 15	1Ah	Section 13.16
1Ah	P_WND_LSB	R/W	00h	Pressure/altitude window LSB [1][3]	No	Pressure/altitude window value bits 0 to 7	1Bh	Section 13.16
1Bh	T_WND	R/W	00h	Temperature window register [1][3]	No	Temperature window value	1Ch	Section 13.17
1Ch	P_MIN_MSB	R/W	00h	Minimum pressure data out MSB [1][3]	No	Minimum pressure/altitude bits 12 to 19	1Dh	Section 13.18
1Dh	P_MIN_CSB	R/W	00h	Minimum pressure data out CSB [1][3]	No	Minimum pressure/altitude bits 4 to 11	1Eh	Section 13.18

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Register Address	Name	Access	Reset value	Description	Reset when STBY to Active	Comment	Auto-increment address	Reference
1Eh	P_MIN_LSB	R/W	00h	Minimum pressure data out LSB [1][3]	No	Minimum pressure/altitude bits 0 to 3	1Fh	Section 13.18
1Fh	T_MIN_MSB	R/W	00h	Minimum temperature data out MSB [1][3]	No	Minimum temperature bits 8 to15	20h	Section 13.20
20h	T_MIN_LSB	R/W	00h	Minimum temperature data out LSB [1][3]	No	Minimum temperature bits 0 to 7	21h	Section 13.20
21h	P_MAX_MSB	R/W	00h	Maximum pressure data out MSB [1][3]	No	Maximum pressure/ altitude bits 12 to 19	22h	Section 13.19
22h	P_MAX_CSB	R/W	00h	Maximum pressure data out CSB [1][3]	No	Maximum pressure/ altitude bits 4 to 11	23h	Section 13.19
23h	P_MAX_LSB	R/W	00h	Maximum pressure data out LSB [1][3]	No	Maximum pressure/ altitude bits 0 to 3	24h	Section 13.19
24h	T_MAX_MSB	R/W	00h	Maximum temperature data out MSB [1][3]	No	Maximum temperature bits 8 to 15	25h	Section 13.21
25h	T_MAX_LSB	R/W	00h	Maximum temperature data out LSB [1][3]	No	Maximum temperature bits 0 to 7	26h	Section 13.21
26h	CTRL_REG1	R/W	00h	Control register 1 [1][4]	No	Modes, oversampling	27h	Section 13.22.1
27h	CTRL_REG2	R/W	00h	Control register 2 [1]	No	Acquisition time step	28h	Section 13.22.2
28h	CTRL_REG3	R/W	00h	Control register 3 [1][4]	No	Interrupt pin configuration	29h	Section 13.22.3
29h	CTRL_REG4	R/W	00h	Control register 4 [1][4]	No	Interrupt enables	2Ah	Section 13.22.4
2Ah	CTRL_REG5	R/W	00h	Control register 5 [1][4]	No	Interrupt output pin assignment	2Bh	Section 13.22.5
2Bh	OFF_P	R/W	00h	Pressure data user offset register	No	Pressure data offset	2Ch	Section 13.23
2Ch	OFF_T	R/W	00h	Temperature data user offset register	No	Temperature data offset	2Dh	Section 13.23.2
2Dh	OFF_H	R/W	00h	Altitude data user offset register	No	Altitude data offset	0Ch	Section 13.23.3

[1] Register contents are preserved when transitioning from ACTIVE to STANDBY mode
[2] Register contents are reset when transitioning from STANDBY to ACTIVE mode.
[3] Register contents can be modified anytime in STANDBY or ACTIVE mode.
[4] Modification of this register's contents can only occur when device in STANDBY mode except the SBYB, OST and RST bit fields in CTRL_REG1 register.

Table 11. Register address map: Area A (F_Mode = 0, FIFO disabled)

Register Address	Name	Access	Reset value	Description	Reset when STBY to Active	Comment	Auto-increment address		Reference
00h/06h	DR_STATUS [1]	R	00h	Sensor status register	Yes	DR_STATUS	01h		Section 13.2
01h	OUT_P_MSB [1]	R	00h	Pressure data out MSB	Yes	Bits12 to 19 of 20-bit real-time pressure sample. Root pointer to pressure and temperature FIFO data.	02h	01h	Section 13.3
02h	OUT_P_CSB [1]	R	00h	Pressure data out CSB	Yes	Bits 4 to 11 of 20-bit real-time pressure sample	03h		Section 13.3
03h	OUT_P_LSB [1]	R	00h	Pressure data out LSB	Yes	Bits 0 to 3 of 20-bit real-time pressure sample	04h		Section 13.3
04h	OUT_T_MSB [1]	R	00h	Temperature data out MSB	Yes	Bits 4 to 11 of 12-bit real-time temperature sample	05h		Section 13.4
05h	OUT_T_LSB [1]	R	00h	Temperature data out LSB	Yes	Bits 0 to 3 of 12-bit real-time temperature sample	00h		Section 13.4

[1] The Registers in Area A from 00h to 05h depend on the F_MODE bit setting in FIFO Setup Register (F_SETUP).
- F_MODE = 00, FIFO is disabled.
- F_MODE = 01 is circular buffer.
- F_MODE = 10 is full stop mode.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Table 12. Register address map: Area A (F_Mode > 0, FIFO in circular buffer or full stop mode)

Register Address	Name	Access	Reset value	Description	Reset when STBY to Active	Comment	Auto-increment address	Reference
00h/0Dh	F_STATUS [1]	R	00h	Sensor status register	Yes	F_STATUS	01h	Section 13.8.1
01h	F_DATA[1]	R	00h	FIFO 8-bit data access	Yes	—	01h	Section 13.8.2
02h	Read to reserved area returns 00 [1]	—	00h	—	n.a.	—	03h	—
03h	Read to reserved area returns 00 [1]	—	00h	—	n.a.	—	04h	—
04h	Read to reserved area returns 00 [1]	—	00h	—	n.a.	—	05h	—
05h	Read to reserved area returns 00 [1]	—	00h	—	n.a.	—	00h	—

[1] The registers in area A from 00h to 05h depend on the F_MODE bit setting in FIFO setup register (F_SETUP).
- F_MODE = 00, FIFO is disabled.
- F_MODE = 01 is circular buffer.
- F_MODE = 10 is full stop mode.

13.1 STATUS - sensor status register (address 00h)

The aliases allow the STATUS register to be read easily before reading the current pressure/altitude or temperature data, the delta pressure/altitude or temperature data, or the FIFO data, using the register address auto-incrementing mechanism.

Table 13. Alias for DR_Status (06h) or F_Status (0Dh) registers

FIFO data enabled mode bit setting	Status register alias
F_MODE = 00 [1]	00h = DR_STATUS (06h)
F_MODE >00	00h = F_STATUS (0Dh)

[1] The F_MODE is defined in Section 13.8.3 " F_SETUP- FIFO setup register (address 0Fh)"

13.2 DR_STATUS - status register (address 06h)

The DR_STATUS register provides the acquisition status information on a per sample basis, and reflects real-time updates to the OUT_P and OUT_T registers. The same STATUS register can be read through an alternate address 00h (F_Mode = 00).

Table 14. DR_STATUS - status register (address 06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PTOW	POW	TOW	reserved	PTDR	PDR	TDR	reserved
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Table 15. DR_STATUS - status register (address 06h) bit description

Bit	Symbol	Description
7	PTOW [1]	Pressure/altitude or temperature data overwrite. PTOW is set to 1 whenever new data is acquired before completing the retrieval of the previous set. This event occurs when the content of at least one data register (OUT_P, OUT_T) has been overwritten. PTOW is cleared when the high-bytes of the data (OUT_P_MSB or OUT_T_MSB) are read, when F_MODE is zero. PTOW is cleared by reading F_DATA register when F_MODE > 0. **0** — No data overwrite has occurred (reset value) **1** — Previous pressure/altitude or temperature data was overwritten by new pressure/altitude or temperature data before it was read
6	POW [2]	Pressure/altitude data overwrite. POW is set to 1 whenever a new pressure/altitude acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. POW is cleared anytime OUT_P_MSB register is read, when F_MODE is zero. POW is cleared by reading F_DATA register when F_MODE > 0. **0** — No data overwrite has occurred (reset value) **1** — Previous pressure/altitude data was overwritten by new pressure/altitude data before it was read
5	TOW[3]	Temperature data overwrite. TOW is set to 1 whenever a new temperature acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. TOW is cleared anytime OUT_T_MSB register is read, when F_MODE is zero. TOW is cleared by reading F_DATA register when F_MODE > 0. **0** — No data overwrite has occurred (reset value) **1** — Previous temperature data was overwritten by new temperature data before it was read
4	reserved	This bit is reserved
3	PTDR [1]	Pressure/altitude or temperature data ready. PTDR signals that a new acquisition for either pressure/altitude or temperature is available. PTDR is cleared anytime OUT_P_MSB or OUT_T_MSB register is read, when F_MODE is zero. PTDR is cleared by reading F_DATA register when F_MODE > 0. **0** — No new set of data ready (reset value) **1** — A new set of data is ready
2	PDR [2]	Pressure/altitude new data available. PDR is set to 1 whenever a new pressure/altitude data acquisition is completed. PDR is cleared anytime OUT_P_MSB register is read, when F_MODE is zero. PDR is cleared by reading F_DATA register when F_MODE > 0. **0** — No new pressure/altitude data is available (reset value) **1** — A new set of Pressure/Altitude data is ready
1	TDR [3]	Temperature new data available. TDR is set to 1 whenever a temperature data acquisition is completed. TDR is cleared anytime OUT_T_MSB register is read, when F_MODE is zero. TDR is cleared by reading F_DATA register when F_MODE > 0. **0** — No new temperature data ready (reset value) **1** — A new temperature data is ready
0	reserved	This bit is reserved

[1] PTDR and PTOW flag generation requires the DREM event flag generator to be enabled in the PT data configuration register (PT_DATA_CFG).
[2] PDR and POW flag generation is required for the pressure/altitude event flag generator to be enabled (PDEFE = 1) in the PT data configuration register (PT_DATA_CFG).
[3] TDR and TOW flag generation is required for the temperature event flag generator to be enabled (TDEFE = 1) in the PT data configuration register (PT_DATA_CFG).

13.2.1 Data registers with F_MODE = 00 (FIFO disabled)

When the FIFO data output register, F_DATA (0Eh), is disabled (F_MODE[7:6] = 00 in the F_SETUP register, 0Fh), the pressure and altitude data registers indicate the real-

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

time status information of the sample data. This data can be either altimeter or barometer data based on the mode defined by the ALT bit in the CTRL_REG1 register. See Section 13.8 "FIFO setup registers" for additional information.

13.3 OUT_P_MSB, OUT_P_CSB, OUT_P_LSB - pressure and altitude data registers (address 01h, 02h, 03h)

Pressure and altitude data registers 01h, 02h and 03h comprise the pressure and altitude data depending on the setting of the ALT bit in the CTRL_REG1 register, in either altimeter or barometer mode. For example if the ALT bit is set (ALT = 1) then after acquisition the data stored in registers 01h, 02h and 03h is the altitude in meters. Otherwise the data stored in registers 01h, 02h and 03h (ALT = 0) is pressure data in Pascals.

The altitude data is stored as a 20-bit signed integer with a fractional part. The OUT_P_MSB (01h) and OUT_P_CSB (02h) registers contain the integer part in meters and the OUT_P_LSB (03h) register contains the fractional part. This value is represented as a Q16.4 fixed-point format where there are 16 integer bits (including the signed bit) and four fractional bits.

The pressure data is stored as a 20-bit unsigned integer with a fractional part. The OUT_P_MSB (01h), OUT_P_CSB (02h) and bits 7 to 6 of the OUT_P_LSB (03h) registers contain the integer part in Pascals. Bits 5 to 4 of OUT_P_LSB contain the fractional component. This value is representative as a Q18.2 fixed point format where there are 18 integer bits (including the signed bit) and two fractional bits.

Note: *When a RAW bit is set in the CTRL_REG1 register then the RAW value is stored in all 24 bits of OUT_P_MSB, OUT_P_CSB and OUT_P_LSB registers whether in altimeter or barometer mode.*

Table 16. OUT_P_MSB, OUT_P_CSB, OUT_P_LSB - pressure and altitude data registers (address 01h, 02h, 03h) bit allocation

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
01h	OUT_P_MSB	PD[19:12]							
02h	OUT_P_CSB	PD[11:4]							
03h	OUT_P_LSB	PD[3:0]				reserved			
Reset		0	0	0	0	0	0	0	0
Access		R	R	R	R	R	R	R	R

13.3.1 Data registers with F_MODE = 00

The DR_STATUS, OUT_P_MSB, OUT_P_CSB, OUT_P_LSB, OUT_T_MSB, and OUT_T_LSB registers are stored in the auto-incrementing address range of 00h to 05h. This allows the host controller to read the status register followed by the 20-bit pressure/altitude and 12-bit temperature in a 6-byte I^2C transaction.

See Section 13.8 "FIFO setup registers" for additional information.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

13.4 OUT_T_MSB, OUT_T_LSB - temperature data registers (address 04h, 05h)

The temperature data is stored as a signed 12-bit integer with a fractional part. The OUT_T_MSB (04h) register contains the integer part in °C and the OUT_T_LSB (05h) register contains the fractional part. This value is representative as a Q8.4 fixed point format where there are eight integer bits (including the signed bit) and four fractional bits.

Note: *When the RAW bit is set in CTRL_REG1 is selected then the RAW temperature value is stored in all 16 bits of the OUT_T_MSB and OUT_T_LSB.*

Table 17. OUT_T_MSB, OUT_T_LSB - temperature data registers (address 04h, 05h) bit allocation

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
04h	OUT_T_MSB	TD[11:4]							
05h	OUT_T_LSB	TD[3:0]				reserved			
Reset		0	0	0	0	0	0	0	0
Access		R	R	R	R	R	R	R	R

13.5 OUT_P_DELTA_MSB, OUT_P_DELTA_CSB, OUT_P_DELTA_LSB - pressure and altitude delta register (address 07h, 08h, 09h)

The pressure and altitude delta registers 07h, 08h and 09h comprise the pressure and altitude delta data and provide the differences from either the last pressure or altitude samples based on the setting of the ALT bit in the CTRL_REG1 register. Device can be in either altimeter or barometer mode.

The altitude data is arranged as a 20-bit signed integer with a fractional part. Stored as meters with the 16 bits of OUT_P_DELTA_MSB and OUT_P_DELTA_CSB and with fractions of a meter stored in four bits in position 7 to 4 of OUT_P_DELTA_LSB.

The pressure is arranged as a 20-bit unsigned integer with a fractional part in Pascals. The first 18 bits are located in OUT_P_DELTA_MSB, OUT_P_DELTA_CSB and bits 7 to 6 of OUT_P_DELTA_LSB. The two bits in position 5 to 4 of OUT_P_DELTA_LSB represent the fractional component.

In RAW mode, these registers are not used and their values are not updated.

Note: *The OUT_P_DELTA register store the difference data information regardless of the state of the FIFO data output register driver bit, F_MODE > 00.*

Table 18. OUT_P_DELTA_MSB, OUT_P_DELTA_CSB, OUT_P_DELTA_LSB - pressure and altitude delta register (address 07h, 08h, 09h) bit allocation

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
07h	OUT_P_DELTA_MSB	PDD[19:12]							
08h	OUT_P_DELTA_CSB	PDD[11:4]							
09h	OUT_P_DELTA_LSB	PDD[3:0]				reserved			
Reset		0	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Location	Bit							
Address	Register	7	6	5	4	3	2	1	0
Access		R	R	R	R	R	R	R	R

13.6 OUT_T_DELTA_MSB, OUT_T_DELTA_LSB - temperature delta register (address 0Ah, 0Bh)

The temperature delta register 0Ah and 0Bh comprise the temperature delta data and provide the difference from the last temperature samples.

The temperature data is arranged as 12-bit signed integer with a fractional part in °C. The eight bits of OUT_T_DELTA_MSB representing degrees and with fractions of a degree stored in four bits in position 7 to 4 of OUT_T_DELTA_LSB.

In RAW mode, these registers are not used and their values are not updated.

Note: *The OUT_T_DELTA register store the difference data information regardless of the state of the FIFO data output register driver bit, F_MODE > 00.*

Table 19. OUT_T_DELTA_MSB, OUT_T_DELTA_LSB - temperature delta register (address 0Ah, 0Bh) bit allocation

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
0Ah	OUT_T_DELTA_MSB	TDD[11:4]							
0Bh	OUT_T_DELTA_LSB	TDD[3:0]				reserved			
Reset		0	0	0	0	0	0	0	0
Access		R	R	R	R	R	R	R	R

13.7 WHO_AM_I - device ID register (address 0Ch)

This register contains the device identifier which is set to C4h by default. The value is factory programmed. Consult the NXP factory for custom alternate values.

Table 20. WHO_AM_I - device ID register (address 0Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WHO_AM_I[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	NVM data 1	NVM data 1	NVM data 0	NVM data 0	NVM data 0	NVM data 1	NVM data 0	NVM data 0

13.8 FIFO setup registers

13.8.1 F_STATUS - FIFO status register (address 0Dh)

Table 21. F_STATUS - FIFO status register (address 0Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	F_OVF	F_WMRK_FLAG	F_CNT[5:0]					

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 22. F_STATUS - FIFO status register (address 0Dh) bit description

F_OVF	F_WMRK_FLAG	Event description
0	—	No FIFO overflow events detected.
1	—	FIFO overflow event detected.
—	**0**	No FIFO watermark events detected.
—	**1**	FIFO watermark event detected. FIFO sample count greater than watermark value

The F_OVF and F_WMRK_FLAG flags remain asserted while the event source is still active, but the user can clear the FIFO interrupt bit flag in the interrupt source register (INT_SOURCE) by reading the F_STATUS register. Therefore, the F_OVF bit flag will remain asserted while the FIFO has overflowed and the F_WMRK_FLAG bit flag will remain asserted while the F_CNT value is greater than then F_WMRK value.

Table 23. F_STATUS - FIFO status register (address 0Dh) bit description

Bit	Symbol	Description
5 to 0	F_CNT	FIFO sample counter. F_CNT[5:0] bits indicate the number of samples currently stored in the FIFO buffer. **00_0000 —** indicates that the FIFO is empty (reset value) **00_0001 to 10_0000 —** indicates 1 to 32 samples stored in FIFO

13.8.2 F_DATA - FIFO data register (address 0Eh)

F_DATA is a read only address which provides access to 8-bit FIFO data. FIFO holds a maximum of 32 samples, a maximum of 5 × 32 = 160 data bytes of samples can be read. When F_MODE bit in FIFO SETUP (F_SETUP) register is set to logic '1', the F_DATA pointer shares the same address location as OUT_P_MSB (01h), therefore all accesses of the FIFO buffer data use the I^2C address 01h. Reads from the other data registers (02h, 03h, 04h, 05h) will return a value of 00h.

Note: *The FIFO will NOT suspend to data accumulation during read transactions to F_DATA.*

Table 24. F_DATA - FIFO data register (address 0Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	F_DATA[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Table 25. Read accesses through F_DATA

1st read	OUT_P_MSB (oldest)
2nd read	OUT_P_CSB (oldest)
3rd read	OUT_P_LSB (oldest)
4th read	OUT_T_MSB (oldest)
5th read	OUT_T_LSB (oldest)
. . .	. . .
	OUT_T_LSB (oldest)
	00h
	00h

13.8.3 F_SETUP- FIFO setup register (address 0Fh)

A FIFO sample count exceeding the watermark event does not stop the FIFO from accepting new data.

The FIFO update rate is dictated by the selected system acquisition rate (ST bits of CTRL_REG2).

When a byte is read from the FIFO buffer the oldest sample data in the FIFO buffer is returned and also deleted from the front of the FIFO buffer, while the FIFO sample count is decremented by one. It is assumed that the host application shall use the I^2C BURST read transaction to dump the FIFO.

Table 26. F_SETUP- FIFO setup register (address 0Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	F_MODE[1:0]		F_WMRK[5:0]					
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Table 27. F_SETUP- FIFO setup register (address 0Fh) bit description

Bit	Symbol	Description
7 to 6	F_MODE[7:6] [1][2]	FIFO buffer overflow mode. **00 —** FIFO is disabled (reset value) **01 —** FIFO contains the most recent samples when overflowed (circular buffer). Oldest sample is discarded to be replaced by new sample **10 —** FIFO stops accepting new samples when overflowed **11 —** Not used The FIFO is flushed whenever the FIFO is disabled, or transitioning from STANDBY mode to ACTIVE mode. Disabling the FIFO (F_MODE = 00) resets the F_OVF, F_WMRK_FLAG, F_CNT to zero. A FIFO overflow event (as when F_CNT = 32) will assert the F_OVF flag and a FIFO sample count equal to the sample count watermark (F_WMRK) asserts the F_WMRK_FLAG event flag. To switch between FIFO modes, first disable the FIFO and then write the new value to F_MODE.
5 to 0	F_WMRK[5:0][3]	FIFO event sample count watermark. These bits set the number of FIFO samples required to trigger a watermark interrupt. A FIFO watermark event flag (F_WMRK_FLAG) is raised when FIFO sample count F_CNT[5:0] value is equal to the F_ WMRK[5:0] watermark. **00_0000 —** FIFO is disabled (reset value) Setting the F_WMRK[5:0] to 00_0000 will disable the FIFO watermark event flag generation.

[1] This bit field can be written in ACTIVE mode.
[2] This bit field can be written in STANDBY mode.
[3] The FIFO mode (F_MODE) cannot be switched between the two operational modes (01 and 10).

13.9 TIME_DLY - time delay register (address 10h)

The time delay register contains the number of ticks of data sample time since the last byte of the FIFO was written. This register starts to increment on FIFO overflow or data wrap and clears when the last byte of FIFO is read.

Table 28. TIME_DLY - time delay register (address 10h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TD[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

13.10 SYSMOD - system mode register (address 11h)

Table 29. SYSMOD - system mode register (address 11h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							SYSMOD
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 30. SYSMOD - system mode register (address 11h) bit description

Bit	Symbol	Description
7 to 1	reserved	These bits are reserved and will always read 0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Bit	Symbol	Description
0	SYSMOD	System mode **0 —** STANDBY mode (reset value) **1 —** ACTIVE mode

13.11 INT_SOURCE - system interrupt status register (address 12h)

The interrupt source register bits that are set (logic '1') to indicate which function has asserted its interrupt and conversely, bits that are cleared (logic '0') indicate which function has not asserted its interrupt.

The setting of the bits is rising edge sensitive, the bit is set by a low to high state change and reset by reading the appropriate source register.

Table 31. INT_SOURCE - system interrupt status register (address 12h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SRC_DRDY	SRC_FIFO	SRC_PW	SRC_TW	SRC_PTH	SRC_TTH	SRC_PCHG	SRC_TCHG
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 32. INT_SOURCE - system interrupt status register (address 12h) bit description

Bit	Symbol	Description
7	SRC_DRDY	Data ready interrupt status bit. Logic '1' indicates that pressure/altitude or temperature data ready interrupt is active indicating the presence of new data and/or a data overwrite, otherwise it is a logic '0'. This bit is asserted when the PTOW and/or PTDR is set and the functional block interrupt has been enabled. This bit is cleared by reading the STATUS and pressure/temperature register.
6	SRC_FIFO	FIFO interrupt status bit. Logic '1' indicates that a FIFO interrupt event such as an overflow event has occurred. FIFO interrupt event generators: FIFO overflow, or (watermark: F_CNT = F_WMRK). **0 —** no FIFO interrupt event has occurred. (reset value) This bit is cleared by reading the F_STATUS register. **1 —** A FIFO interrupt event such as an overflow event has occurred.
5	SRC_PW	Altitude/pressure alerter status bit near or equal to target pressure/altitude (near is within target value ± window value). **0 —** (reset value) Window value needs to be non zero for interrupt to trigger.
4	SRC_TW	Temperature alerter status bit near or equal to target temperature (near is within target value ± window value.) **0 —** (reset value) Window value needs to be non zero for interrupt to trigger.
3	SRC_PTH	Altitude/pressure threshold interrupt. **0 —** If the window is set to 0, it will only trigger on crossing the center threshold. (reset value) **1 —** With the window set to a non zero value, the trigger will occur on crossing any of the thresholds: upper, center or lower.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Bit	Symbol	Description
2	SRC_TTH	Temperature threshold interrupt. **0 —** If the window is set to 0, it will only trigger on crossing the center threshold.(reset value) **1 —** With the window set to a non zero value, the trigger will occur on crossing any of the thresholds: upper, center or lower.
1	SRC_PCHG	Delta P interrupt status bit. **0 —** (reset value)
0	SRC_TCHG	Delta T interrupt status bit. **0 —** (reset value)

13.12 PT_DATA_CFG - sensor data register (address13h)

The PT_DATA_CFG register configures the pressure data, temperature data and event flag generator.

Table 33. PT_DATA_CFG - sensor data register (address13h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved					DREM	PDEFE	TDEFE
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 34. PT_DATA_CFG - sensor data register (address13h) bit description

Bit	Symbol	Description
7 to 3	reserved	These bits are reserved
2	DREM	Data ready event mode. **0 —** Event detection disabled (reset value) If the DREM bit is cleared logic '0' and one or more of the data ready event flags are enabled, then an event flag will be raised whenever the system acquires a new set of data. **1 —** Generate data ready event flag on new pressure/altitude or temperature data. If the DREM bit is set logic '1' and one or more of the data ready event flags (PDEFE, TDEFE) are enabled, then an event flag will be raised upon change in state of the data.
1	PDEFE	Data event flag enable on new pressure/altitude **0 —** Event detection disabled (reset value) **1 —** Raise event flag on new pressure/altitude data
0	TDEFE	Data event flag enable on new temperature data. **0 —** Event detection disabled (reset value) **1 —** Raise event flag on new temperature data

13.13 BAR_IN_MSB, BAR_IN_LSB - barometric pressure input register (address 14h, 15h)

Barometric input for altitude calculations. Input is equivalent to sea level pressure for measurement location. Value is input in two Pa units.

Units are input as unsigned 16-bit integers. The default value is 101,326 Pa. The default value can be changed by writing to this register.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Table 35. BAR_IN_MSB, BAR_IN_LSB - barometric pressure input register (address 14h, 15h) bit allocation

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
14h	BAR_IN_MSB	BAR[15:8]							
15h	BAR_IN_LSB	BAR[7:0]							
Reset MSB		1	1	0	0	0	1	0	1
Reset LSB		1	1	1	0	0	1	1	1
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.14 P_TGT_MSB, P_TGT_LSB - pressure/altitude target value register (address 16h, 17h)

Altitude or pressure target value.

Depending on the setting of the ALT bit in the CTRL_REG1 register, in operates in either altimeter or barometer mode. This value works in conjunction with the window value (P_WND_MSB and P_WND_LSB). In altitude mode, the register value is 16-bit signed integer in meters.

In pressure mode, the value is a 16-bit unsigned value in two Pa units.

Table 36. P_TGT_MSB, P_TGT_LSB - pressure/altitude target value register (address 16h, 17h) bit allocation

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
16h	P_TGT_MSB	P_TGT[15:8]							
17h	P_TGT_LSB	P_TGT[7:0]							
Reset		0	0	0	0	0	0	0	0
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.15 T_TGT- temperature target value register (address 18h)

Temperature target value is input as an 8-bit signed integer in °C.

Table 37. T_TGT- temperature target value register (address 18h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	T_TGT[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.16 P_WND_LSB, P_WND_MSB - pressure/altitude window value register (address 19h, 1Ah)

Pressure or altitude window value register is arranged as an unsigned 16-bit integer of window value in meters or in two Pa units, depending on either altimeter or barometer mode.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Table 38. P_WND_LSB, P_WND_MSB - pressure/altitude window value register (address 19h, 1Ah) bit allocation

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
19h	P_WND_LSB	P_W[15:8]							
1Ah	P_WND_MSB	P_W[7:0]							
Reset		0	0	0	0	0	0	0	0
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.17 T_WIN- temperature window value register (address 18h)

The temperature alarm window value register is an unsigned 8-bit value in °C.

Table 39. T_WIN- temperature window value register (address 18h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	T_WIN[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.18 P_MIN_MSB, P_MIN_CSB, P_MIN_LSB - minimum pressure or altitude register (address 1Ch, 1Dh, 1Eh)

Register with captured minimum pressure or altitude value.

The altitude data is arranged as a 20-bit signed integer in meters. The first 16 bits are located in P_MIN_MSB and P_MIN_CSB. Fractions of a meter are stored in four bits in position 7 to 4 of P_MIN_LSB.

The pressure is arranged as a 20-bit unsigned data in Pascals. The first 18 bits are located in P_MIN_MSB, P_MIN_CSB and bits 7 to 6 of P_MIN_LSB. The two bits in position 5 to 4 of P_MIN_LSB represent the fractional component.

The register is cleared on power-up or manually by writing '0' to the register.

Table 40. P_MIN_MSB, P_MIN_CSB, P_MIN_LSB - minimum pressure or altitude register (address 1Ch, 1Dh, 1Eh) bit allocation

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1Ch	P_MIN_MSB	P_MIN[19:12]							
1Dh	P_MIN_CSB	P_MIN[11:4]							
1Eh	P_MIN_LSB	P_MIN[3:0]				reserved			
Reset		0	0	0	0	0	0	0	0
Access MSB		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Access CSB		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Access LSB		R/W	R/W	R/W	R/W	R	R	R	R

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

13.19 P_MAX_MSB, P_MAX_CSB, P_MAX_LSB - maximum pressure or altitude register (address 21h, 22h, 23h)

Register with captured maximum pressure or altitude value.

The altitude data is arranged as a 20-bit signed integer in meters. The first 16 bits are located in P_MAX_MSB and P_MAX_CSB. Fractions of a meter stored in four bits in position 7 to 4 of P_MAX_LSB.

The pressure is arranged as a 20-bit unsigned data in Pascals. The first 18 bits are located in P_MAX_MSB, P_MAX_CSB and bits 7 to 6 of P_MAX_LSB. The two bits in position 5 to 4 of P_MAX_LSB represent the fractional component.

The register is cleared on power-up or manually by writing '0' to the registers.

Table 41. P_MAX_MSB, P_MAX_CSB, P_MAX_LSB - maximum pressure or altitude register (address 21h, 22h, 23h) bit allocation

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
21h	P_MAX_MSB	P_MAX[19:12]							
22h	P_MAX_CSB	P_MAX[11:4]							
23h	P_MAX_LSB	P_MAX[3:0]				reserved			
Reset		0	0	0	0	0	0	0	0
Access MSB		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Access CSB		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Access LSB		R/W	R/W	R/W	R/W	R	R	R	R

13.20 T_MIN_MSB, T_MIN_LSB - minimum temperature register (address 1Fh, 20h)

Register with captured minimum temperature value.

The temperature data is arranged as a 12-bit signed integer in °C. The first eight bits are located in T_MIN_MSB with fractions of a degree stored in four bits in position 7 to 4 of T_MIN_LSB.

The register is cleared on power-up or manually by writing '0' to the registers.

Table 42. T_MIN_MSB, T_MIN_LSB - minimum temperature register (address 1Fh, 20h) bit allocation

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1Fh	T_MIN_MSB	T_MIN[11:4]							
20h	T_MIN_LSB	T_MIN[3:0]				reserved			
Reset		0	0	0	0	0	0	0	0
Access MSB		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Access LSB		R/W	R/W	R/W	R/W	R	R	R	R

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

13.21 T_MAX_MSB, T_MAX_LSB - maximum temperature register (address 24h, 25h)

Register with captured maximum temperature value.

The temperature data is arranged as a 12-bit signed integer in °C. The first eight bits are located in T_MAX_MSB with fractions of a degree stored in four bits in position 7 to 4 of T_MAX_LSB.

The register is cleared on power-up or manually by writing '0' to the registers

Table 43. T_MAX_MSB, T_MAX_LSB - minimum temperature register (address 24h, 25h) bit allocation

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
24h	T_MAX_MSB	T_MAX[11:4]							
25h	T_MAX_LSB	T_MAX[3:0]				reserved			
Reset		0	0	0	0	0	0	0	0
Access MSB **Access** LSB		R/W R/W	R/W R/W	R/W R/W	R/W R/W	R/W R	R/W R	R/W R	R/W R

13.22 Control registers

13.22.1 CTRL_REG1 - control register 1 (address 26h)

Note: *Except for STANDBY and OST mode selection, the device must be in STANDBY mode to change any of the fields within bits 7 to 0 of CTRL_REG1 (26h).*

Table 44. CTRL_REG1 - control register 1 (address 26h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ALT	RAW	OS[2:0]			0 (R) RST (W)	OST	SBYB
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 45. CTRL_REG1 - control register 1 (address 26h) bit description

Bit	Symbol	Description
7	ALT	Altimeter/barometer mode. **0 —** Part is in barometer mode (reset value) **1 —** Part is in altimeter mode
6	RAW	RAW output mode. RAW bit will output ADC data with no post processing, except for oversampling. No scaling or offsets will be applied in the digital domain. The FIFO must be disabled and all other functionality including alarms, deltas, and other interrupts are disabled.
5 to 3	OS[2:0]	Oversample ratio. These bits select the oversampling ratio. Value is 2^{OS}. The default value is 000 for a ratio of 1.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Bit	Symbol	Description
2	0 (R) RST (W)	Software reset. This bit is used to activate the software reset. The boot mechanism can be enabled in STANDBY and ACTIVE mode. When the boot bit is enabled the boot mechanism resets all functional block registers and loads the respective internal registers with default values. If the system was already in STANDBY mode, the reboot process will immediately begin, or else if the system was in ACTIVE mode, the boot mechanism will automatically transition the system from ACTIVE mode to STANDBY mode. Only then can the reboot process begin. The I^2C communication system is reset to avoid accidental corrupted data access. At the end of the boot process the RST bit is de-asserted to 0. Reading this bit will return a value of zero. **0 —** Device reset disabled (reset value) **1 —** Device reset enabled
1	OST	OST bit will initiate a measurement immediately. If the SBYB bit is set to active, setting the OST bit will initiate an immediate measurement, the part will then return to acquiring data as per the setting of the ST bits in CTRL_REG2. In this mode, the OST bit does not clear itself and must be cleared and set again to initiate another immediate measurement. In one-shot mode, when SBYB is 0, the OST bit is an auto-clear bit. When OST is set, the device initiates a measurement by going into active mode. Once a pressure/altitude and temperature measurement is completed, it clears the OST bit and comes back to STANDBY mode. User shall read the value of the OST bit before writing to this bit again.
0	SBYB	This bit is sets the mode to ACTIVE, where the system will make measurements at periodic times based on the value of ST bits. **0 —** Part is in STANDBY mode (reset value) **1 —** Part is ACTIVE

Table 46. System output sample rate selection

OS2	OS1	OS0	Oversample ratio	Minimum time between data samples
0	0	0	1	6 ms
0	0	1	2	10 ms
0	1	0	4	18 ms
0	1	1	8	34 ms
1	0	0	16	66 ms
1	0	1	32	130 ms
1	1	0	64	258 ms
1	1	1	128	512 ms

Note: *The RAW bit overrides the ALT mode and writes uncompensated pressure and temperature data.*

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

13.22.2 CTRL_REG2 - control register 2 (address 27h)

Table 47. CTRL_REG2 - control register 2 (address 27h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		LOAD_OUTPUT	ALARM_SEL	ST[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 48. CTRL_REG2 - control register 2 (address 27h) bit description

Bit	Symbol	Description
7 to 6	reserved	These bits are reserved.
5	LOAD_OUTPUT	This is to load the target values for SRC_PW/SRC_TW and SRC_PTH/SRC_TTH. **0 —** Do not load OUT_P/OUT_T as target values (reset value) **1 —** The next values of OUT_P/OUT_T are used to set the target values for the interrupts. ***Notes:*** • *This bit must be set at least once if ALARM_SEL=1* • *To reload the next OUT_P/OUT_T as the target values, clear and set again.*
4	ALARM_SEL	The bit selects the target value for SRC_PW/SRC_TW and SRC_PTH/SRC_TTH. **0 —** (reset value) The values in P_TGT_MSB, P_TGT_LSB and T_TGT are used. **1 —** The values in OUT_P/OUT_T are used for calculating the interrupts SRC_PW/SRC_TW and SRC_PTH/SRC_TTH.
3 to 0	ST[3:0]	Auto acquisition time step. **0 —** (reset value) **Step value is 2^{ST} —** Giving a range of 1 second to 215 seconds (9 hours)

13.22.3 CTRL_REG3 - interrupt CTRL register (address 28h)

Table 49. CTRL_REG3 - interrupt CTRL register (address 28h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		IPOL1	PP_OD1	reserved		IPOL2	PP_OD2
Reset	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R	R	R/W	R/W

Table 50. CTRL_REG3 - interrupt CTRL register (address 28h) bit description

Bit	Symbol	Description
7 to 6	reserved	These bits are reserved.
5	IPOL1	The IPOL bit selects the polarity of the interrupt signal. When IPOL is '0' (default value) any interrupt event will signalled with a logical '0'. Interrupt Polarity active high, or active low on interrupt pad INT1. **0 —** Active low (reset value) **1 —** Active high

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Bit	Symbol	Description
4	PP_OD1	This bit configures the interrupt pin to push-pull or in open drain mode. The default value is 0 which corresponds to push-pull mode. The open drain configuration can be used for connecting multiple interrupt signals on the same interrupt line. push-pull/open drain selection on interrupt pad INT1. **0 —** Internal pullup (reset value) **1 —** Open drain
3 to 2	reserved	These bits are reserved.
1	PP_OD2	Interrupt polarity active high, or active low on interrupt pad INT2. **0 —** Active low (reset value) **1 —** Active high
0	PP_OD2	Push-pull/open drain selection on interrupt pad INT2. **0 —** Internal pullup (reset value) **1 —** Open drain

13.22.4 CTRL_REG4 - interrupt enable register (address 29h)

The corresponding functional block interrupt enable bit allows the functional block to route its event detection flags to the system's interrupt controller. The interrupt controller routes the enabled functional block interrupt to the INT1 or INT2 pin.

Table 51. CTRL_REG4 - interrupt enable register (address 29h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	INT_EN_DRDY	INT_EN_FIFO	INT_EN_PW	INT_EN_TW	INT_EN_PTH	INT_EN_TTH	INT_EN_PCHG	INT_EN_TCHG
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 52. CTRL_REG4 - interrupt enable register (address 29h) bit description

Bit	Symbol	Description
7	INT_EN_DRDY	Interrupt enable. **0 —** Data ready interrupt disabled (reset value) **1 —** Data ready interrupt enabled
6	INT_EN_FIFO	Interrupt enable. **0 —** FIFO interrupt disabled (reset value) **1 —** FIFO interrupt enabled
5	INT_EN_PW	Interrupt enable. **0 —** Pressure window interrupt disabled (reset value) **1 —** Pressure window interrupt enabled
4	INT_EN_TW	Interrupt enable. **0 —** Temperature window interrupt disabled (reset value) **1 —** Temperature window interrupt enabled
3	INT_EN_PTH	Interrupt enable. **0 —** Pressure threshold interrupt disabled (reset value) **1 —** Pressure threshold interrupt enabled

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Bit	Symbol	Description
2	INT_EN_TTH	Interrupt enable. **0** — Temperature threshold interrupt disabled (reset value) **1** — Temperature threshold interrupt enabled
1	INT_EN_PCHG	Interrupt enable. **0** — Pressure change interrupt disabled (reset value) **1** — Pressure change interrupt enabled
0	INT_EN_TCHG	Interrupt enable. **0** — Temperature change interrupt disabled (reset value) **1** — Temperature change interrupt enabled

13.22.5 CTRL_REG5 - interrupt configuration register (address 2Ah)

Table 53. CTRL_REG5 - interrupt configuration register (address 2Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	INT_CFG_DRDY	INT_CFG_FIFO	INT_CFG_PW	INT_CFG_TW	INT_CFG_PTH	INT_CFG_TTH	INT_CFG_PCHG	INT_CFG_TCHG
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 54. CTRL_REG5 - interrupt configuration register (address 2Ah) bit description

Bit	Symbol	Description
7	INT_EN_DRDY	INT1/INT2 configuration. **0** — Interrupt is routed to INT2 pin (reset value) **1** — Interrupt is routed to INT1
6	INT_CFG_FIFO	INT1/INT2 configuration. **0** — Interrupt is routed to INT2 pin (reset value) **1** — Interrupt is routed to INT1
5	INT_CFG_PW	INT1/INT2 configuration. **0** — Interrupt is routed to INT2 pin (reset value) **1** — Interrupt is routed to INT1
4	INT_CFG_TW	INT1/INT2 configuration. **0** — Interrupt is routed to INT2 pin (reset value) **1** — Interrupt is routed to INT1
3	INT_CFG_PTH	INT1/INT2 configuration. **0** — Interrupt is routed to INT2 pin (reset value) **1** — Interrupt is routed to INT1
2	INT_CFG_TTH	INT1/INT2 configuration. **0** — Interrupt is routed to INT2 pin (reset value) **1** — Interrupt is routed to INT1
1	INT_CFG_PCHG	INT1/INT2 configuration. **0** — Interrupt is routed to INT2 pin (reset value) **1** — Interrupt is routed to INT1

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Bit	Symbol	Description
0	INT_CFG_TCHG	INT1/INT2 configuration. **0 —** Interrupt is routed to INT2 pin (reset value) **1 —** Interrupt is routed to INT1

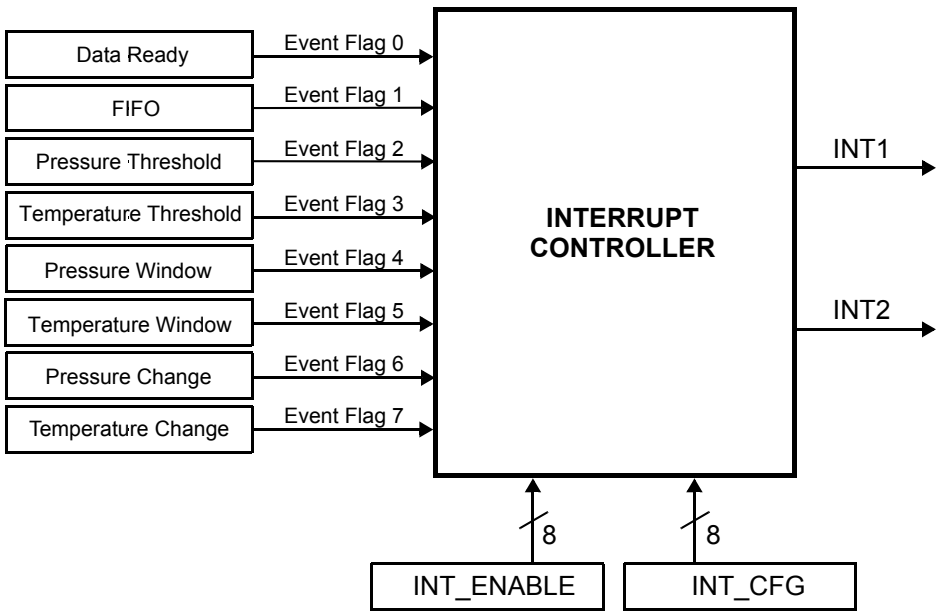


Figure 9. Interrupt controller block diagram

The system's interrupt controller uses the corresponding bit field in the CTRL_REG5 register to determine the routing table for the INT1 and INT2 interrupt pins. If the bit value is logic '0' the functional block's interrupt is routed to INT2, and if the bit value is logic '1' then the interrupt is routed to INT1.

All interrupts routed to INT1 or INT2 are logically OR'd as illustrated in Figure 10. One or more functional blocks can assert an interrupt pin simultaneously, therefore a host application responding to an interrupt should read the INT_SOURCE register to determine the appropriate sources of the interrupt.

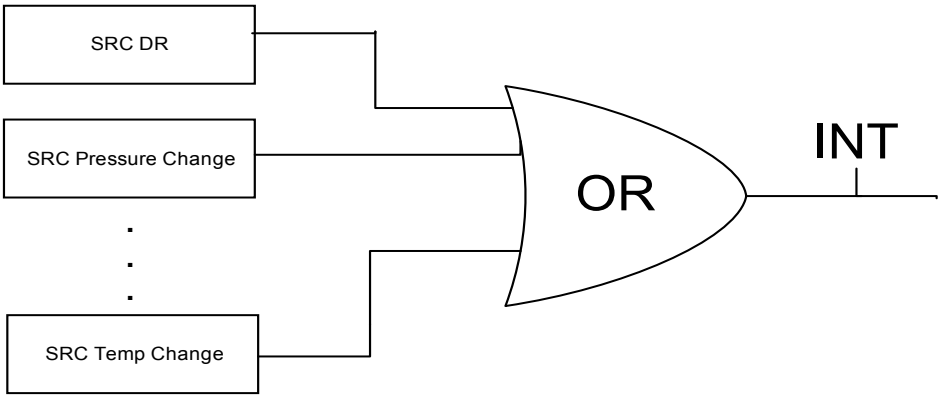


Figure 10. INT1/INT2 pin control logic

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

13.23 Offset correction registers

The 2's complement offset correction registers values are used to trim the temperature, altitude and pressure offsets that might occur over the life of the product.

13.23.1 OFF_P - offset pressure correction register (address 2Bh)

Pressure user accessible offset trim value expressed as an 8-bit, 2's complement number. The user offset registers may be adjusted to enhance accuracy and optimize the system performance. Range is from −512 to +508 Pa, 4 Pa/LSB.

Table 55. OFF_P - offset correction register (address 2Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFF_P[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.23.2 OFF_T - offset temperature correction register (address 2Ch)

Temperature user accessible offset trim value expressed as an 8-bit, 2's complement number. The user offset registers may be adjusted to enhance accuracy and optimize the system performance. Range is from −8 to +7.9375 °C, 0.0625 °C/LSB.

Table 56. OFF_P - offset temperature correction register (address 2Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFF_T[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.23.3 OFF_H - altitude data user offset register (address 2Dh)

Altitude data user offset register (OFF_H) is expressed as a 2's complement number in meters. See Section 8.1.3 "Pressure/altitude". The user offset register provides user adjustment to the vertical height of the altitude output. The range of values are from −128 to +127 meters.

Table 57. OFF_H - altitude data user offset register (address 2Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OFF_H[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

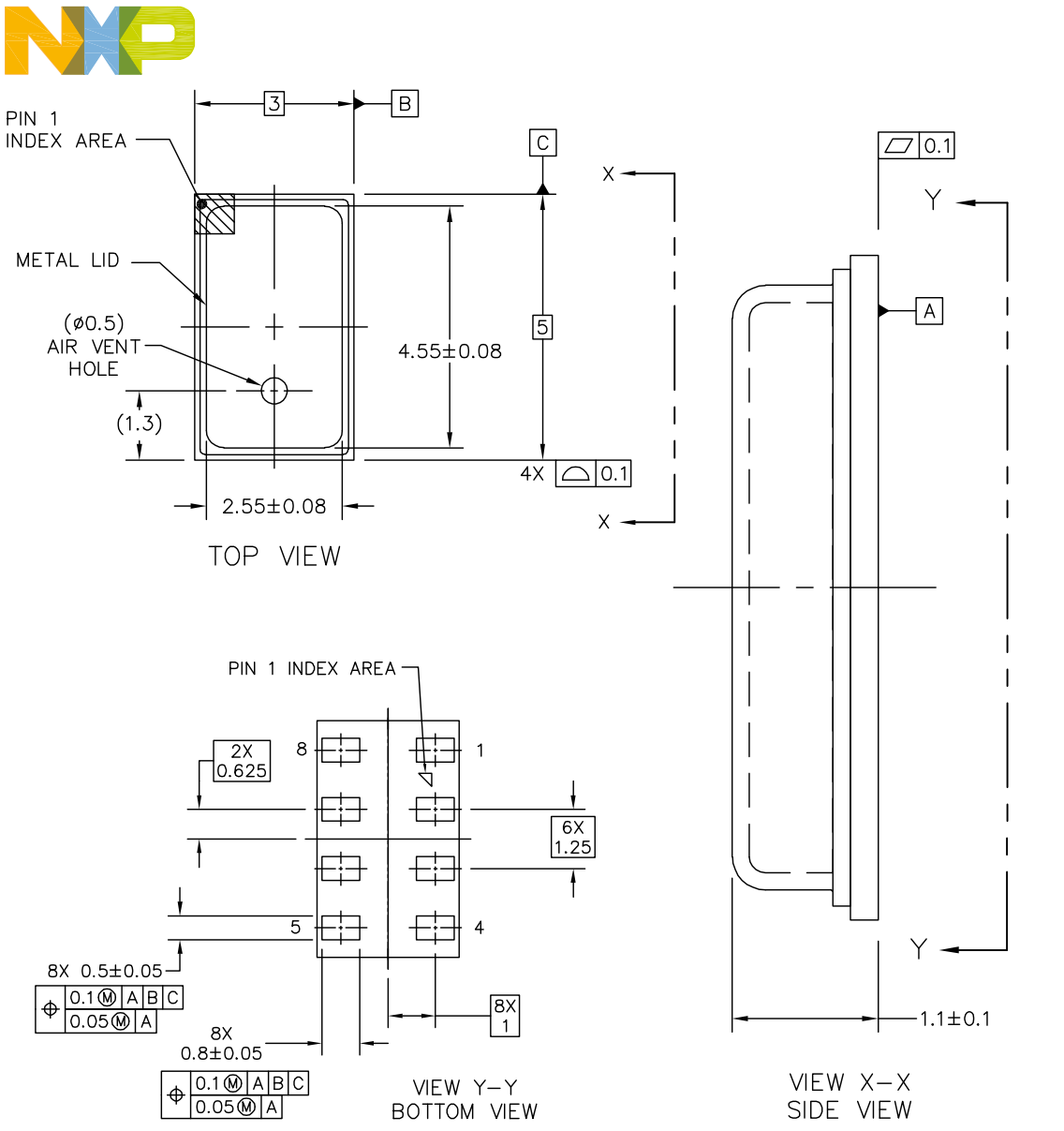
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

14 Package information

14.1 Package dimensions

This drawing is located at http://nxp.com/files/shared/doc/package_info/98ASA00260D.pdf.



All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

3. STYLE:
   PIN 1: VDD PIN 5: INT2
   PIN 2: CAP PIN 6: INT1
   PIN 3: GND PIN 7: SDA
   PIN 4: VDDIO PIN 8: SCL

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LGA 8 I/O, 3 X 5 X 1.25 PITCH, SENSOR 1.2MAX MM PKG	DOCUMENT NO: 98ASA00260D	REV: A
	STANDARD: NON–JEDEC	
	SOT1768–1	07 JAN 2016

Figure 11. Case 98ASA00260D, LGA package

15 Soldering/landing pad information

The LGA package is compliant with the RoHS standard.

Note: *Pin 1 index area marker does not have any internal electrical connections. Handling and soldering recommendations for pressure sensors are available in application notes AN1984 and AN3150.*

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

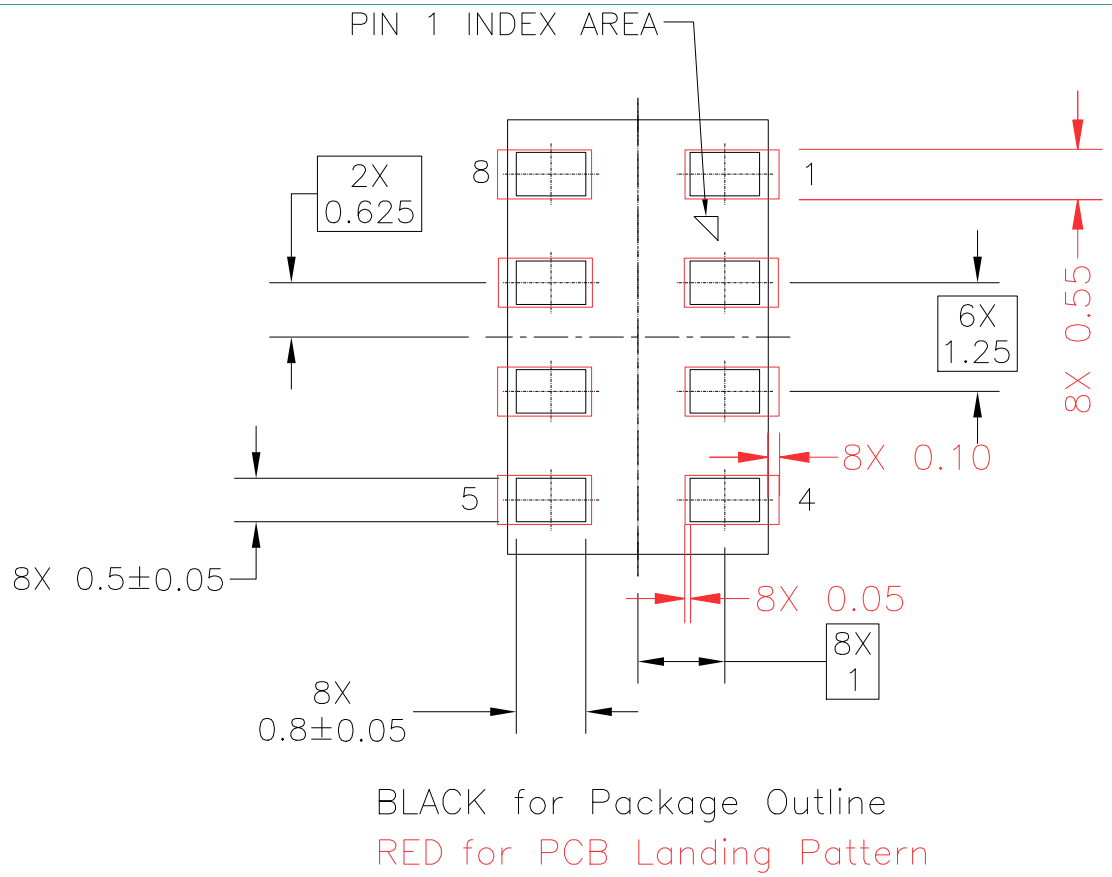
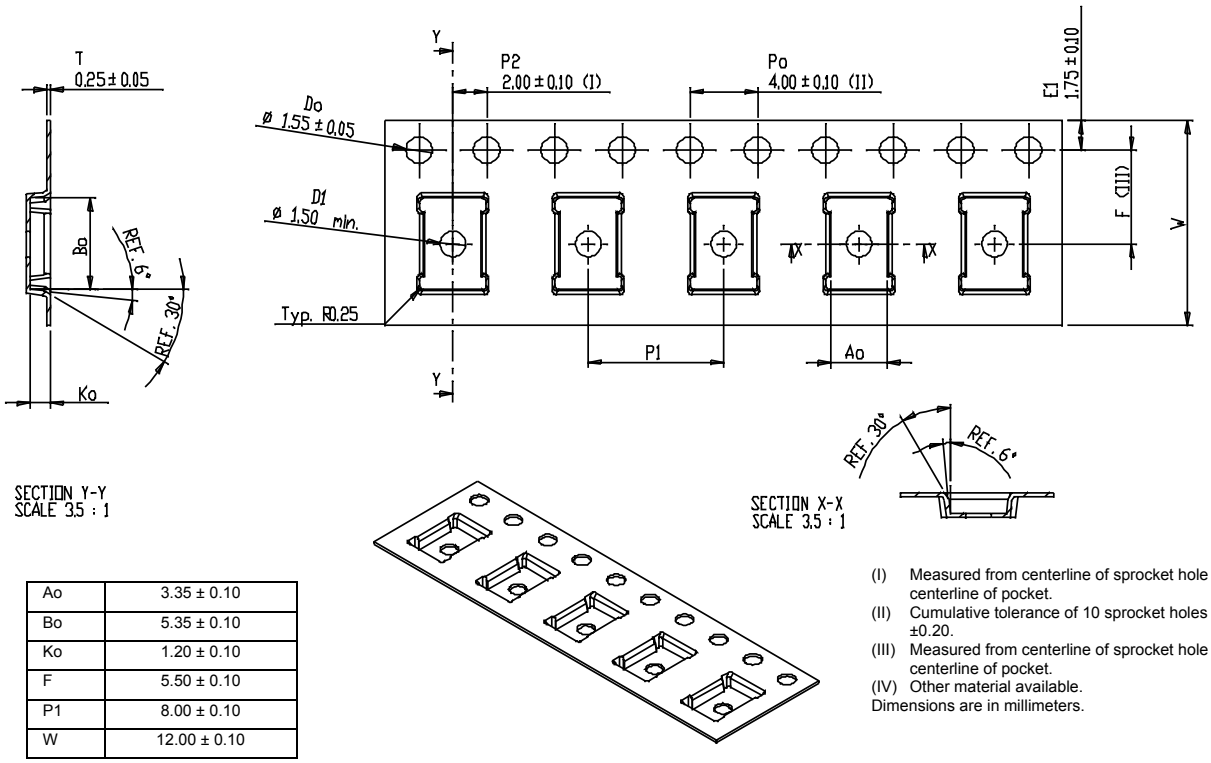


Figure 12. Recommended PCB landing pattern

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

16 Tape and reel specifications



Ao	3.35 ± 0.10
Bo	5.35 ± 0.10
Ko	1.20 ± 0.10
F	5.50 ± 0.10
P1	8.00 ± 0.10
W	12.00 ± 0.10

(I) Measured from centerline of sprocket hole to centerline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ±0.20.
(III) Measured from centerline of sprocket hole to centerline of pocket.
(IV) Other material available.
Dimensions are in millimeters.

Figure 13. LGA 3 mm × 5 mm embossed carrier tape dimensions

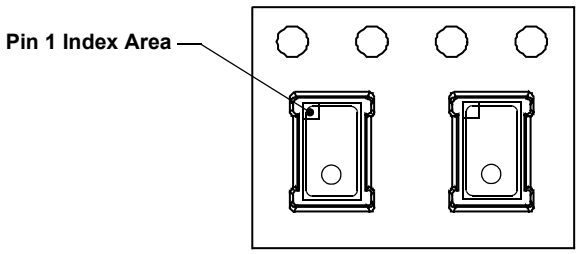


Figure 14. Device orientation in chip carrier

17 Related documentation

The device features and operations may be described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

- Go to the product page at nxp.com/MPL3115A2.
- Click on the **Documentation** tab.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

18 Revision history

Table 58. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MPL3115A2 v.5.1	20160913	Technical data	n.a.	MPL3115A2 v.5.0
Modifications	• Maximum ratings table correction, T_{OP}, value is –40 to 85 °C. • Mechanical characteristics table correction, pressure/altitude resolution in barometer mode unit is Pa. • Mechanical characteristics table correction, pressure/altitude resolution in altimeter mode unit is m.			
MPL3115A2 v.5.0	20160816	Technical data	n.a.	MPL3115A2 v.4.0
MPL3115A2 v.4.0	2015 September	Technical data	n.a.	MPL3115A2 v.3.0
MPL3115A2 v.3.0	2013 December	Advanced information	n.a.	MPL3115A2 v.2.2
MPL3115A2 v.2.2	2012 July	Advanced information	n.a.	MPL3115A2 v.2.1
MPL3115A2 v.2.1	2012 May	Advanced information	n.a.	MPL3115A2 v.2.0
MPL3115A2 v.2.0	2012 April	Advanced information	n.a.	MPL3115A2 v.1.0
MPL3115A2 v.1.0	2011 December	Product preview	n.a.	MPL3115A2 v.0
MPL3115A2 v.0	2011 June	Product preview	n.a.	n.a.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

19 Legal information

19.1 Data sheet status

Document status[1]	Product status[2]	Definition
Data sheet: Product preview	Development	This document contains certain information on a product under development. NXP reserves the right to change or discontinue this product without notice.
Data sheet: Advance information	Qualification	This document contains information on a new product. Specifications and information herein are subject to change without notice.
Data sheet: Technical data	Production	NXP Semiconductors reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

19.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

19.3 Disclaimers

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in NXP data sheets and/ or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/salestermsandconditions.

19.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — is a trademark of NXP B.V.

the NXP logo — is a trademark of NXP B.V.

Freescale — is a trademark of NXP B.V.

the Freescale logo — is a trademark of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Tables

Tab. 1. Ordering information 2
Tab. 2. Pin description 3
Tab. 3. Maximum ratings 6
Tab. 4. ESD and latchup protection characteristics 6
Tab. 5. Mechanical characteristics 6
Tab. 6. Electrical characteristics 7
Tab. 7. Serial interface pin descriptions 9
Tab. 8. I2C Slave timing values 9
Tab. 9. Mode of operation description 11
Tab. 10. Register address map 18
Tab. 11. Register address map: Area A (F_Mode = 0, FIFO disabled) 19
Tab. 12. Register address map: Area A (F_Mode > 0, FIFO in circular buffer or full stop mode) 20
Tab. 13. Alias for DR_Status (06h) or F_Status (0Dh) registers 20
Tab. 14. DR_STATUS - status register (address 06h) bit allocation 20
Tab. 15. DR_STATUS - status register (address 06h) bit description 21
Tab. 16. OUT_P_MSB, OUT_P_CSB, OUT_P_LSB - pressure and altitude data registers (address 01h, 02h, 03h) bit allocation 22
Tab. 17. OUT_T_MSB, OUT_T_LSB - temperature data registers (address 04h, 05h) bit allocation 23
Tab. 18. OUT_P_DELTA_MSB, OUT_P_DELTA_CSB, OUT_P_DELTA_LSB - pressure and altitude delta register (address 07h, 08h, 09h) bit allocation 23
Tab. 19. OUT_T_DELTA_MSB, OUT_T_DELTA_LSB - temperature delta register (address 0Ah, 0Bh) bit allocation 24
Tab. 20. WHO_AM_I - device ID register (address 0Ch) bit allocation 24
Tab. 21. F_STATUS - FIFO status register (address 0Dh) bit allocation 24
Tab. 22. F_STATUS - FIFO status register (address 0Dh) bit description 25
Tab. 23. F_STATUS - FIFO status register (address 0Dh) bit description 25
Tab. 24. F_DATA - FIFO data register (address 0Eh) bit allocation 25
Tab. 25. Read accesses through F_DATA 26
Tab. 26. F_SETUP- FIFO setup register (address 0Fh) bit allocation 26
Tab. 27. F_SETUP- FIFO setup register (address 0Fh) bit description 27
Tab. 28. TIME_DLY - time delay register (address 10h) bit allocation 27
Tab. 29. SYSMOD - system mode register (address 11h) bit allocation 27
Tab. 30. SYSMOD - system mode register (address 11h) bit description 27
Tab. 31. INT_SOURCE - system interrupt status register (address 12h) bit allocation 28
Tab. 32. INT_SOURCE - system interrupt status register (address 12h) bit description 28
Tab. 33. PT_DATA_CFG - sensor data register (address13h) bit allocation 29
Tab. 34. PT_DATA_CFG - sensor data register (address13h) bit description 29
Tab. 35. BAR_IN_MSB, BAR_IN_LSB - barometric pressure input register (address 14h, 15h) bit allocation 30
Tab. 36. P_TGT_MSB, P_TGT_LSB - pressure/ altitude target value register (address 16h, 17h) bit allocation 30
Tab. 37. T_TGT- temperature target value register (address 18h) bit allocation 30
Tab. 38. P_WND_LSB, P_WND_MSB - pressure/ altitude window value register (address 19h, 1Ah) bit allocation 31
Tab. 39. T_WIN- temperature window value register (address 18h) bit allocation 31
Tab. 40. P_MIN_MSB, P_MIN_CSB, P_MIN_LSB - minimum pressure or altitude register (address 1Ch, 1Dh, 1Eh) bit allocation 31
Tab. 41. P_MAX_MSB, P_MAX_CSB, P_MAX_LSB - maximum pressure or altitude register (address 21h, 22h, 23h) bit allocation 32
Tab. 42. T_MIN_MSB, T_MIN_LSB - minimum temperature register (address 1Fh, 20h) bit allocation 32
Tab. 43. T_MAX_MSB, T_MAX_LSB - minimum temperature register (address 24h, 25h) bit allocation 33
Tab. 44. CTRL_REG1 - control register 1 (address 26h) bit allocation 33
Tab. 45. CTRL_REG1 - control register 1 (address 26h) bit description 33
Tab. 46. System output sample rate selection 34
Tab. 47. CTRL_REG2 - control register 2 (address 27h) bit allocation 35
Tab. 48. CTRL_REG2 - control register 2 (address 27h) bit description 35
Tab. 49. CTRL_REG3 - interrupt CTRL register (address 28h) bit allocation 35
Tab. 50. CTRL_REG3 - interrupt CTRL register (address 28h) bit description 35
Tab. 51. CTRL_REG4 - interrupt enable register (address 29h) bit allocation 36
Tab. 52. CTRL_REG4 - interrupt enable register (address 29h) bit description 36
Tab. 53. CTRL_REG5 - interrupt configuration register (address 2Ah) bit allocation 37
Tab. 54. CTRL_REG5 - interrupt configuration register (address 2Ah) bit description 37
Tab. 55. OFF_P - offset correction register (address 2Bh) bit allocation 39

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Tab. 56. OFF_P - offset temperature correction register (address 2Ch) bit allocation 39
Tab. 57. OFF_H - altitude data user offset register (address 2Dh) bit allocation 39
Tab. 58. Revision history 44

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Figures

Fig. 1. Block diagram 2
Fig. 2. 8-pin LGA pinout 3
Fig. 3. Typical application diagram 3
Fig. 4. I2C slave timing diagram 10
Fig. 5. I2C bus transmission signals 11
Fig. 6. Mode transition diagram 11
Fig. 7. Polling - no FIFO 13
Fig. 8. Interrupt - no FIFO 14
Fig. 9. Interrupt controller block diagram 38
Fig. 10. INT1/INT2 pin control logic 38
Fig. 11. Case 98ASA00260D, LGA package 40
Fig. 12. Recommended PCB landing pattern 42
Fig. 13. LGA 3 mm × 5 mm embossed carrier tape dimensions 43
Fig. 14. Device orientation in chip carrier 43

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

Contents

1 General description 1
2 Features and benefits 1
3 Applications 2
4 Ordering information 2
5 Block diagram 2
6 Pinning information 3
6.1 Pinning 3
6.2 Pin description 3
7 System connections 3
8 Mechanical and electrical specifications 4
8.1 Terminology 4
8.1.1 Resolution 4
8.1.2 Accuracy 4
8.1.2.1 Offset 4
8.1.2.2 Linearity 4
8.1.2.3 Absolute pressure 5
8.1.2.4 Span 5
8.1.3 Pressure/altitude 5
8.2 Absolute maximum ratings 5
8.3 Mechanical characteristics 6
8.4 Electrical characteristics 7
9 Digital interface 9
9.1 I2C characteristics 9
9.2 I2C operation 10
10 Modes of operation 11
10.1 OFF 12
10.2 STANDBY 12
10.3 ACTIVE 12
11 Quick start setup 12
12 Functionality 15
12.1 Factory calibration 15
12.2 Barometer/altimeter function 15
12.2.1 Barometric input 15
12.3 Temperature function 16
12.4 Autonomous data acquisition 16
12.5 FIFO 16
12.6 External interrupts 16
12.6.1 Reach target threshold pressure/altitude (SRC_PTH) 16
12.6.2 Reach window target pressure/altitude (SRC_PW) 16
12.6.3 Reach target threshold temperature (SRC_TTH) 17
12.6.4 Reach window target temperature (SRC_TW) 17
12.6.5 Pressure/altitude change (SRC_PCHG) 17
12.6.6 Temperature change (SRC_TCHG) 17
12.6.7 Data ready 17
12.6.8 FIFO event 17
12.6.9 Pressure/altitude and temperature delta 17
12.6.10 Min/max data value storage 17
13 Register descriptions 18
13.1 STATUS - sensor status register (address 00h) 20
13.2 DR_STATUS - status register (address 06h) ... 20
13.2.1 Data registers with F_MODE = 00 (FIFO disabled) 21
13.3 OUT_P_MSB, OUT_P_CSB, OUT_P_LSB - pressure and altitude data registers (address 01h, 02h, 03h) 22
13.3.1 Data registers with F_MODE = 00 22
13.4 OUT_T_MSB, OUT_T_LSB - temperature data registers (address 04h, 05h) 23
13.5 OUT_P_DELTA_MSB, OUT_P_DELTA_CSB, OUT_P_DELTA_LSB - pressure and altitude delta register (address 07h, 08h, 09h) 23
13.6 OUT_T_DELTA_MSB, OUT_T_DELTA_LSB - temperature delta register (address 0Ah, 0Bh) 24
13.7 WHO_AM_I - device ID register (address 0Ch) 24
13.8 FIFO setup registers 24
13.8.1 F_STATUS - FIFO status register (address 0Dh) 24
13.8.2 F_DATA - FIFO data register (address 0Eh) 25
13.8.3 F_SETUP- FIFO setup register (address 0Fh) 26
13.9 TIME_DLY - time delay register (address 10h) 27
13.10 SYSMOD - system mode register (address 11h) 27
13.11 INT_SOURCE - system interrupt status register (address 12h) 28
13.12 PT_DATA_CFG - sensor data register (address13h) 29
13.13 BAR_IN_MSB, BAR_IN_LSB - barometric pressure input register (address 14h, 15h) 29
13.14 P_TGT_MSB, P_TGT_LSB - pressure/ altitude target value register (address 16h, 17h) 30
13.15 T_TGT- temperature target value register (address 18h) 30
13.16 P_WND_LSB, P_WND_MSB - pressure/ altitude window value register (address 19h, 1Ah) 30
13.17 T_WIN- temperature window value register (address 18h) 31
13.18 P_MIN_MSB, P_MIN_CSB, P_MIN_LSB - minimum pressure or altitude register (address 1Ch, 1Dh, 1Eh) 31
13.19 P_MAX_MSB, P_MAX_CSB, P_MAX_LSB - maximum pressure or altitude register (address 21h, 22h, 23h) 32
13.20 T_MIN_MSB, T_MIN_LSB - minimum temperature register (address 1Fh, 20h) 32
13.21 T_MAX_MSB, T_MAX_LSB - maximum temperature register (address 24h, 25h) 33
13.22 Control registers 33
13.22.1 CTRL_REG1 - control register 1 (address 26h) 33

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2016. All rights reserved

13.22.2 CTRL_REG2 - control register 2 (address 27h) 35
13.22.3 CTRL_REG3 - interrupt CTRL register (address 28h) 35
13.22.4 CTRL_REG4 - interrupt enable register (address 29h) 36
13.22.5 CTRL_REG5 - interrupt configuration register (address 2Ah) 37
13.23 Offset correction registers 39
13.23.1 OFF_P - offset pressure correction register (address 2Bh) 39
13.23.2 OFF_T - offset temperature correction register (address 2Ch) 39
13.23.3 OFF_H - altitude data user offset register (address 2Dh) 39
14 Package information 40
14.1 Package dimensions 40
15 Soldering/landing pad information 41
16 Tape and reel specifications 43
17 Related documentation 43
18 Revision history 44
19 Legal information 45

© NXP B.V. 2016. All rights reserved

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com
Released on 13 September 2016

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Freescale Semiconductor:

DEMOSTBMPL3115A2 MPL3115A2R1 MPL3115A2 MPL3115A2T1